博士論文

A Performance Study on ATLAS Level1 Endcap Muon Trigger using 7TeV/c collision data

ATLAS 実験初段エンドキャップミューオントリガーの、7TeV/c における陽子衝突実験の結果に基づく性能に関する研究

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Chapter 1

Introduction

The LHC (Large Hadron Collider)[5] is the largest proton-proton collider overall the world. With 27km circumference of the LHC, this collider can accelerate proton beams upto 7TeV with a designed feature (14TeV collision at Center of Mass system). Experiments at the LHC have started from 2009 with 450 GeV beam energy, and now the beam energy reaches 3.5TeV. ATLAS (A Toroidal Lhc Apparatus)[9], whose detector is installed in one of collision points, is one of experimental project at the LHC. The main purpose of ATLAS is to explore undiscovered particles and new physics phenomena. One of the most important goal is to find the Higgs boson. Standard Model[2][3] predicts the existence of Higgs which has not found yet, in spite of extensive searches by many experiments. In the Standard Model, Higgs takes a role of giving mass to all particles, quarks, leptons and gauge bosons. Higgs is predicted to decay into known particles. Some decay channels contain the high transverse momentum muons in the final state. Muon is a lepton and muon identification is easier than other signals. Measurement system of muon is one of important ingredients of the Higgs search at the LHC.

In the LHC, the rate of proton-proton interaction is estimated to be 1GHz at the design luminosity. On the other hand, the rate of Higgs production is estimated to be about 10^{-1}Hz. We should pick up interesting phenomena which are buried in large number of backgrounds. The trigger system is equipped with ATLAS data taking scheme to pick up interesting events. Three staged processing is adopted for the trigger system, to reduce recording rate to about 200Hz. The first stage of trigger system is named Level 1 (LVL1) Trigger. The LVL1 Trigger is performed by customized electronics for deadtime-less processing within 2.5 us of latency. The LVL1 Trigger consists of calorimeter trigger and muon trigger. An important role of LVL1 Muon Trigger is to find the high transverse momentum

muons. Muon trigger consists of the barrel and endcap parts. Kobe university have been contributed in the development of ATLAS LVL1 Endcap Muon Trigger System; construction of detectors, design of the trigger scheme and electronics, and development of software.

This thesis will present the performance study of LVL1 Endcap Muon Trigger at the center of mass 7TeV. At first, a brief descripton on LHC and ATLAS experiment will be described. Next, the LVL1 Endcap Muon Trigger will be explained. Especially the details of electronics to determine the trigger candidate will be presented. After that, an study of the performance of LVL1 Endcap Muon Trigger is described. Adjustments of the trigger logic, trigger efficiency, and timing studies will be presented. At the end of this thesis, a summary will be presented, and the contributions of LVL1 Endacp Muon Trigger in ATLAS will be demonstrated.

Chapter 2

The LHC

This chapter describes about the Large Hadron Collider (LHC) and introduces their main experiments. LHC is designed for a proton-proton collisions with 14 TeV of center of mass system (CM) energy, which is the highest energy all over the world. Its design luminosity is $10^{34} cm^{-2} sec^{-1}$. Bunch crossing rate is 25 ns and total rate of proton-proton interaction is up to 10^9 per second. Then, LHC can reach at unexplored energy region for new physics studies.

2.1 The LHC Accelerator

The LHC is a synchrotron with 26.7 km circumference, and each bunch of protons is accelerated to 7 TeV/c. Super Proton Synchrotron (SPS) is the injector for the LHC and accelerates 2 GeV/c protons from Proton Synchrotron (PS) to 450 GeV/c. The beamline of the LHC is composed mainly of super-conducting NbTi bending magnets [5] and quadruples for the beam optics, and accelerating cavities. These super-condicting dipole magnets are placed along two separated beamlines and produce magnetic fields of 8.4 T in vertical direction. There are four collision points at the LHC, where the following detectors are placed.

- ATLAS (A Toroidal LHC ApparatusS)
- CMS (Compact Muon Solenoid) [6]
- LHCb [8]
- ALICE (A Large Ion Collider Experiment) [7]

Main Ring Circumference	26658.87m
Proton Energy	7.0 TeV
Injection Energy	450 GeV/c
Bunch Length	77mm
Beam Radius	15.9 μm
Luminosity Lifetime	10 hours
Number of Protons	$1.1 \times 10^{11}/bunch$
Bunch Interval	24.95 ns
Beam Crossing Angle	300μrad

Table 2.1: The Design Parameters of LHC

ATLAS and CMS are general purpose detectors, LHCb is specialized for b-physics and ALICE is for heavy ion collision (1PeV Pb-Pb collision at the maximum energy). Locations of these detectors with respect to the proton rings are shown in Fig 2.1. The design parameters of LHC is listed on Table 2.1.

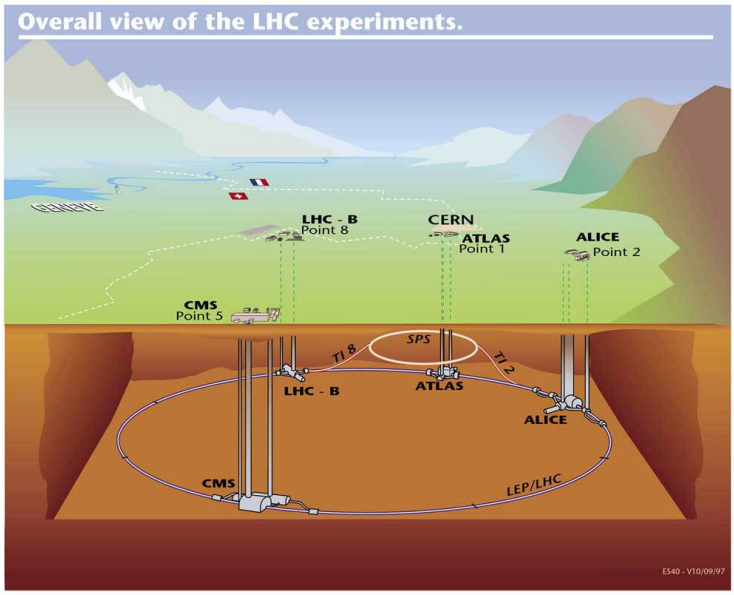

Figure 2.1: Schematic view of the LHC accelerator complex

2.2 Luminosity

One of the important parameters of a collider is the luminosity L. For a physical process with cross-section σ, the event rate $\frac{dN}{dt}$ is given by

$$\frac{dN}{dt} = \sigma \times L \tag{2-2-1}$$

In the case of a proton collider like the LHC, the luminosity is given by;

$$L = \frac{N_{p1} N_{p2} f_{cross}}{4\pi \sigma_x^* \sigma_y^*} \tag{2-2-2}$$

where N_{p1} and N_{p2} are the number of protons of colliding bunches and f_{cross} is the bunch crossing frequency. σ_x^* and σ_y^* are transverse beam size of horizontal(x) and vertical(y) direction at the interaction point respectively and $\sigma_x^* \sigma_y^*$ gives cross section of the beam. It is clear that increase of N_{p1}, N_{p2}, and f_{cross}, and decrease of σ_x^*, σ_y^* result in high luminosity.

At the end of 2011, the peak luminosity have achieved $6 \times 10^{33} cm^{-2} sec^{-1}$.

2.3 Particle Production Rates

As the proton is a composite particle, 14 TeV of CM energy is distributed to partons inside, quarks and gluons. Not only valence quarks but also the gluons holding them together can interact, and additionally, a whole sea of quark-antiquark pairs are allowed a fleeting existence under the law of quantum mechanics as well. Therefore, mass states up to a few TeV can be created. Figure 2.2 shows the prediction of particle-production cross section for the processes at the LHC and Tevatron together with production rate at the $10^{33} cm^{-2} sec^{-1}$. It can be seen that the total cross section is more than ten order of magnitude larger than that of the Higgs production. Therefore, detectors must have capability to handle such an enormous total event rate and distinguish the signals of interest from the other events such as proton-proton inelastic events and minimum bias events (QCD), or backgrounds such as beam halo events and beam gas events.

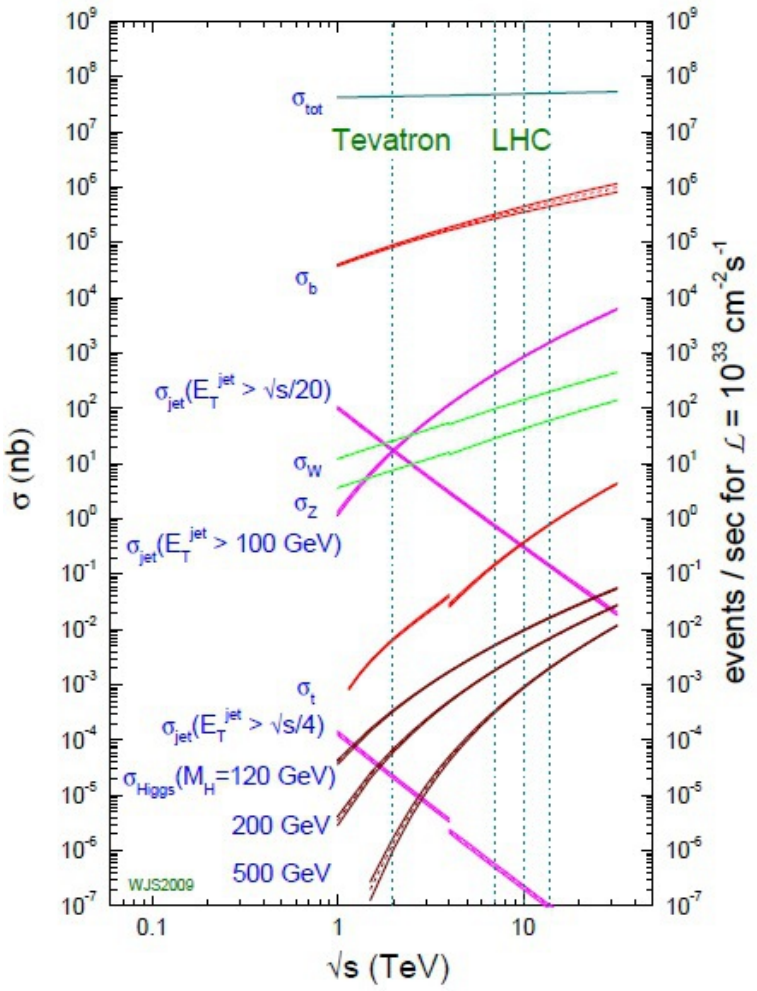

Figure 2.2: Predicted cross section of proton-proton interaction as CM energy. Vertical axis on left side shows production cross section, right side vertical axis shows event rate. The energy at the Tevatron, Fermilab as well as ones at the LHC are indicated.

Chapter 3

Physics Motivation at the ATLAS Experiment

Particle physics deals with the elementary building blocks of matter and their mutual interactions. During the 20th century a theory emerged that succesfully describes all known elementary particles and their interactions. The Standard Model incorporates the Glashow-Weinberg-Salam theory [4] of electro week processes and quantum chromodynamics (QCD). Only the gravitational interactions are not included. The Standard Model is a quantum field theory that describes the interactions of spin $\frac{1}{2}$ point like fermions, whose interactions are mediated by spin 1 gauge bosons. The fermions one, the leptons, and a category of particles that are subjected to the strong interactions, the quarks. Further, they are ordered in three generations of increasing mass, as shown Table 3.1. Each generation consists of two leptons and two quarks, each set with a difference of unit electric charge. The first generation consists of the electron (e), the electron neutrino (ν_e), the up quark (u), and the down quark (d). All these fermions are stable and are the building blocks of ordinary matter. The up and down quarks form protons and neutrons, which together with the electrons build up the atom and subsequently all form of matters surrounded us. The second generation consists of the muon (μ) and muon neutrino (ν_μ), the charm quark (c), and the strange quark (s). These have the same propaties as the first generation particles, except that they have larger masses and are not stable. The particles of the third generation, consisting of tau (τ), the tau neutrino (ν_τ), the top quark (t) and bottom quark (b), are again heavier. The neutrinos are neutral particles, all other particles are charged. Mass and charges for each particles are also summarized in Table 3.1.

In a simple gauge theory, interactions between fermions occur via the exchange of gauge bosons.

	1st generation	2nd generation	3rd generation	charge
Leptons	e (0.511 MeV/c^2)	μ (106 MeV/c^2)	τ (1.78GeV/c^2)	-1
Neutrinos	ν_e	ν_μ	ν_τ	0
Quarks	u (1.5-3.3 MeV/c^2)	c (1.16-1.34 GeV/c^2)	t (169.1-173.3 GeV/c^2)	$+\frac{2}{3}$
	d (3.5-6.0 MeV/c^2)	s (70-130 MeV/c^2)	b (4.13-4.37 GeV/c^2)	$-\frac{1}{3}$

Table 3.1: Matter particles of the Standard Model. Values in brackets indicate their masses.

The electromagnetic force is mediated by the photon (γ). The weak force is mediated via the exchange of either the charged W^+ or W^- boson or the neutral Z boson. The strong force is mediated by the gluon (g). The photon and the gluon are massless, the mass of $W^\pm$ is 80.4 GeV/c^2 and the mass of the Z boson is 91.2 GeV/c^2 [38]. They have been observed in experiments.

While the Standard Model well describes the interactions of the components of matter at the smallest scales (10^{-18}m) and highest energies (about 200 GeV/c^2) accessible to past experiments, there are some problems which have not been solved yet and there need to be theories beyond the Standard Model. In this chapter, especially the Standard Model Higgs [10] is mentioned.

3.1 Standard Model Higgs

In the Standard Model, all gauge bosons are necessarily massless in order to preserve the local gauge invariance of the theory. However, $W^\pm$ and Z bosons have masses. The Higgs mechanism [11][12] provides a possible explanation of the origin of the masses through the spontaneous symmetry breaking of the gauge invariance.

3.1.1 Higgs Mechanism

The Higgs mechanism is an extension of the Goldstone Theorem which states that if a Lagrangian has a global symmetry which is not a symmetry of the vacuum. Then, there must exist one massless boson, scalar or pseudo-scalar, associated to each generator which does not annihilate the vacuum. In the Higgs mechanism, a weak isospin doublet of complex scaler fields $\phi^0(x)$ and $\phi^+(x)$ is introduced as;

$$\phi(x) = \begin{pmatrix} \phi^+(x) \\ \phi^0(x) \end{pmatrix} = \frac{1}{\sqrt{2}} \begin{pmatrix} \phi_1(x) + i\phi_2(x) \\ \phi_3(x) + i\phi_4(x) \end{pmatrix} \tag{3-1-1}$$

It belongs to the $SU(2)_L \otimes U(1)_Y$ multiplets and along with the scalar potential V(ϕ) represented as;

$$V(\phi) = \mu^2\phi^\dagger\phi + \lambda(\phi^\dagger\phi)^2, \lambda > 0 \tag{3-1-2}$$

This gives a contribution to the electroweak Lagrangian L as;

$$L_{Higgs} = (D_\mu\phi)^\dagger(D_\mu\phi) - V(\phi), D^\mu = \delta^\mu - i\frac{g\sigma}{2}\dot{W}^\mu - i\frac{g\prime YB}{2} \tag{3-1-3}$$

whre D_μ is the covariant derivative.

The minimum of V corresponding to the ground state of the system (i.e. vacuum) is at $|\phi|$=0 for the case μ^2 >0, while, for the case μ^2 <0, the minimum shifts to

$$|\phi^2| = \phi\phi^\dagger = \frac{1}{2}(\phi_1^2 + \phi_2^2 + \phi_3^2 + \phi_4^2) = -\frac{\mu^2}{2\lambda} = \frac{v^2}{2} \tag{3-1-4}$$

where v is the vacuum expectation value. This leads to the definition of new field variables, η_1=ϕ_1, η_2=ϕ_2, η_3=ϕ_3-v and η_4=ϕ_4, and the potential takes the form as shown in Figure 3.1. They have their origin at an arbitrarily minimum chosen as;

$$| < 0|\phi|0 > | = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 \\ v \end{pmatrix} \tag{3-1-5}$$

The symmetry of the Lagrangian becomes hidden by the choice of a particular minimum. The Lagrangian expressed in the new fields reveals a massive scaler particle η_2 of mass $\sqrt{2\lambda v^2}$, the Higgs boson H and three massless Goldstone bosons, ϕ_1, ϕ_2, and η_3. These Goldstone bosons can be removed by applying a unitary gauge transformation to $\phi(x)$ such that only the real Higgs field remains like;

$$\phi(x) = U\phi(x) = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 \\ v + H(x) \end{pmatrix} \tag{3-1-6}$$

In this way, the degree of freedom corresponding to the three disappeared Goldstone boson are eaten by the $W^\pm$ and Z fields which acquire mass and a third, longitudinal polarization state. Then,

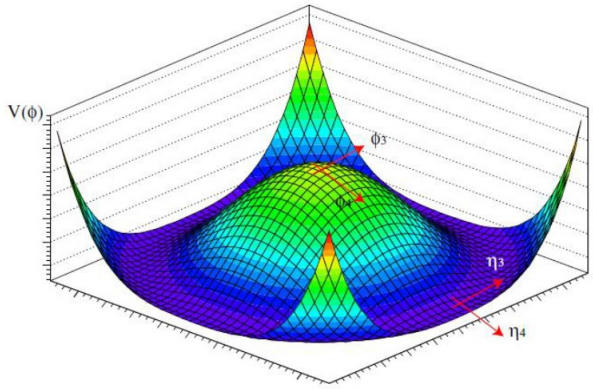

Figure 3.1: Higgs Potential

the gauge boson masses are generated as;

$$M_W = \frac{gv}{2} \tag{3-1-7}$$

$$M_Z = \frac{1}{2}\sqrt{g^2 + g'^2} \tag{3-1-8}$$

$$M_\gamma = 0 \tag{3-1-9}$$

This massive physical field Z_μ and the massless one A_μ are represented using their mixing angle θ_W (called the Weinberg angle) as;

$$A_\mu = cos\theta_W B_\mu + sinW^3_\mu \tag{3-1-10}$$

$$Z_\mu = -sin\theta_W B_\mu + cosW^3_\mu \tag{3-1-11}$$

$$\tag{3-1-12}$$

where the value θ_W satisfies the following equation;

$$\frac{g'}{g} = \tan\theta_W \tag{3-1-13}$$

In addition, the Higgs field couples to the fermion matter fields to generate their masses. The coupling of the Higgs field to a fermion pair is parameterized by an arbitary Yukawa coupling constant $\lambda_f = \frac{m_f\sqrt{2}}{v}$, which is different for each fermion and proportional to its mass m_f. Lepton number conservation is assumed within the SM, giving a diagonal lepton mass matrix. The lack of quark generating number conservation in electroweak interactions means that observed physical mass eigenstates

of quarks are not eigenstates of weak isospin. The level of quark mixing is parameterized in terms of the Cabibbo-Kobayashi-Masukawa mixing matrix.

3.1.2 Experimental Constraint of Higgs Mass

The mas of the Higgs boson remains the only unknown parameter in the Standard Model, and several constraints on its mass have been obtained from past experimental measurements. The most precise bound on the Higgs mass come from the LEP experiments [20]. A Higgs with its mass smaller than 114.4 GeV/c^2 is excluded with a confidence level of 95% by direct searches at LEP. Furthermore an upper limit on its mass can be obtained from a fit to the electroweak results from LEP and SLD. The result of the fit is shown in Figure 3.2. It shows the $\Delta\chi^2(m_H) = \chi^2_{min}(m_H) - \chi^2_{min}$ as a function of the Higgs mass. The mass region that is excluded by direct searches is indicated by the shaded area. The associated band represents the estimate of the theoretical uncertainty due to higher-order corrections. After a renormalization of the probability content of the region $m_H > 114$ GeV/c^2 to 100%, using the assumption that the prior probability density for m_H is flag in m_H, an upper limit of 199GeV/c^2 is obtained with a confidence level of 95 %.

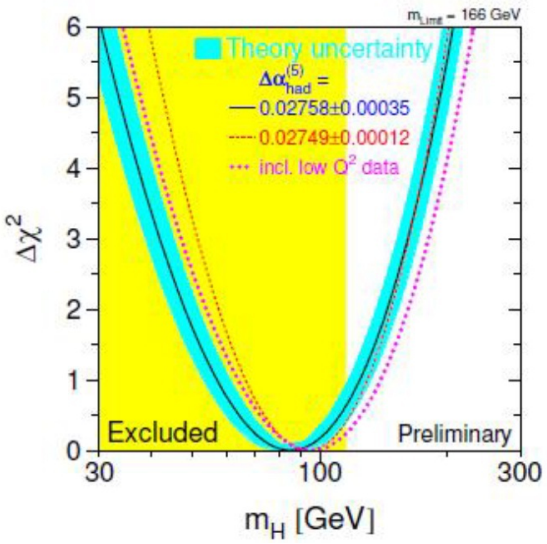

Figure 3.2: $\Delta\chi^2(m_H) = \chi^2_{min}(m_H) - \chi^2_{min}$ as a function of the Higgs mass [13]

3.1.2.1 Higgs Boson Production

Figure 3.3 shows typical Feynman diagrams of Higgs boson production process for the ATLAS experiment. Details for each process are mentioned below.

- $gg \rightarrow H$

  The gluon fusion processes (Figure 3.3-(a)) procceed primarily through a top quark triangle loop, and is the dominant neutral Higgs boson production mechanism at LHC, with crossections of toughly 200 – 0.1 pb for M_{Higgs} = 100 – 1000 GeV/c^2. The dependence of the gluon fusion cross section on different parton densities yields roughly an additional 15 % uncertainty in the theoretical prediction.

- $gg \rightarrow ggV^*V^* \rightarrow qqH$

  The vector boson fusion (VBF, Figure 3.3-(b)) is a shorthand notation for the full $qq \rightarrow qqH$ process, where both quarks radiate virtual vector bosons which then annihirate to produce the Higgs boson. The resulting Standard Model cross section are in the range 5 - 0.001 pb for M_{Higgs} = 100 - 10000 GeV/c^2.

- $q\bar{q} \rightarrow V^* \rightarrow VH$

  The cross section for $q\bar{q} \rightarrow W^{\pm}H$ (Figure 3.3-(c), summed over both W charge states) reaches values of 2 - 0.001 pb for M_{Higgs} = 100 - 1000 GeV/c^2. The corresponding $q\bar{q} \rightarrow ZH$ cross section is roughly a factor of two lower over the same Higgs boson mass range. The theoritical uncertainty is estimated to be about 15% from the remaining scale dependence. The dependence on different sets of parton densities is rather weak and also leads to a variation of the production cross sections by about 15%. The signature of Higgs boson production in the VH channel are governed by the corresponding decays of the Higgs boson and vector boson.

- $gg, qq \rightarrow t\bar{t}H$ Also the process $gg, qq \rightarrow t\bar{t}H$ (Figure 3.3-(d)) is relevant only for small Higgs masses. The analytical expression for the parton cross section, even at lowest order, is quite involved, so that just the final result for the LHC cross section are shown in Figure 3.4.

3.1.3 Higgs Boson Decay and Search at ATLAS

For each Higgs mass, the Standard Model precisely predicts the decay channels of the Higgs and their brunching ratio, which allows a precise assessment of the Higgs boson properties. The decay width of the Higgs boson as a function of Higgs mass is shown in Figure 3.5. Here, Higgs decay process for each Higgs mass M_H are detailed.

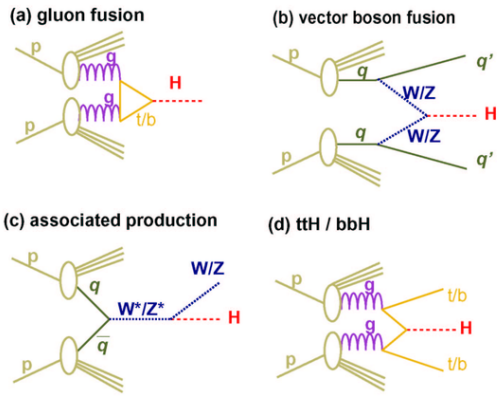

Figure 3.3: Higgs Production

- Low-Mass Higgs Boson ($M_H < 120GeV/c^2$):

  Below the WW or ZZ threshold ($M_H < 2M_Z$), the dominant decay into the heaviest accessible pair of quarks

$$H \to b\bar{b} \tag{3-1-14}$$

  is swamped by the QCD background (the direct $b\bar{b}$ crosssection is very high, see Figure 3.5). The decay channel

$$H \to \gamma\gamma \tag{3-1-15}$$

  suffers an enormous background from $qp \to \gamma\gamma, gg \to \gamma\gamma, gg \to q\gamma\gamma$, and $Z \to e^+e^-$ processes, where the jets or $e^\pm$ fake a γ. These backgrounds can be reduced if the detector is equiped with excellent photon resolution and excellent γ/jet and $\gamma/e^\pm$ separation. Hence an electromagnetic calorimetry with excellent performance is required.

- Search for VBF H $\to \gamma\gamma$ mode:

  When the mass of Higgs is relatively small ($115 < m_{Higgs} < 140GeV/c^2$), a vector boson fusion process with

$$H \to \tau^+\tau^- \tag{3-1-16}$$

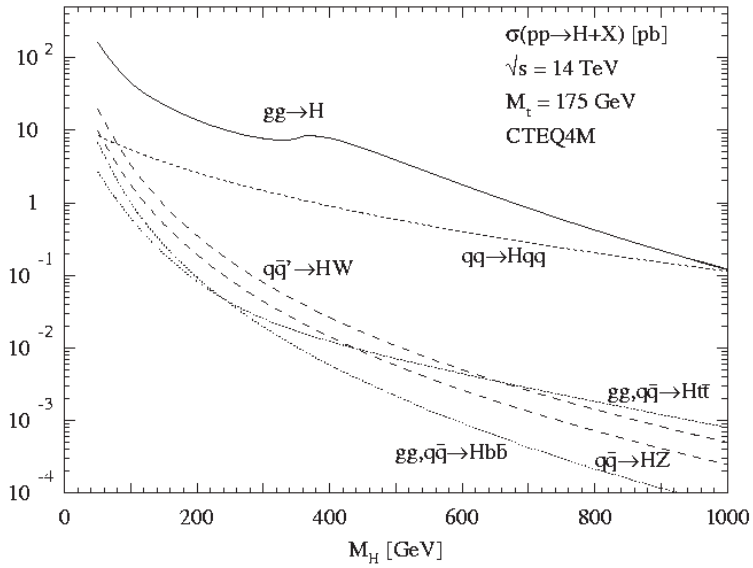

Figure 3.4: Production Crosssection of Higgs [14]

plays a important role for this discovery. In this channel, $\gamma\gamma \rightarrow$ leptonic decay + hadronic decay (lepton-hadron mode) is as important as leptonic decay + leptonic decay (lepton-lepton mode) because a branching ratio of hadronic tau decay is larger than that of leptonic tau decay by a factor of about 2. It leads this channel to the first discovery of Higgs.

Since W and Z bosons are heavy, the outgoing quarks have larger transverse momenta than the QCD background process. They will be observed in a forward region with high-p_T. Tagging these forward jets help us to suppress the background processes. Furthermore, there is no color exchange between two outgoing quarks, the Higgs boson will be observed in large rapidity gap, where activities of QCD jets are small.

$H \rightarrow \tau\tau$ provides high-p_T lepton from a leptonic tau decay and it can be used as a trigger of E_T information.

Dominant background process is Drell-Yan with two high-p_T jets and the invariant mass distribution makes a peak at Z_0 mass.

- Intermediate Mass Higgs Boson ($120GeV/c^2 < M_H < 800GeV/c^2$):

  In this mass region the decay

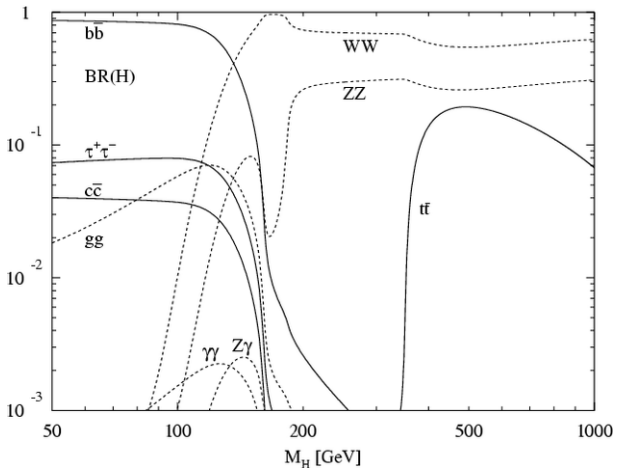

Figure 3.5: Decay width of the Higgs boson as a function of the Higgs mass [14]

$$H \rightarrow ZZ^{(*)} \rightarrow l^+l^-l^+l^- \tag{3-1-17}$$

provides a very clean signature of the Higgs boson. For the range $M_H < 2M_Z$ one of the two Z boson is virtual (off-shell). For a Higgs mass of 150 GeV/c^2 one expects about 550 such events per year in a summing which luminosity. The four leptons have a high transverse momentum ($5GeV/c < p_T < 50GeV/c$). The background is mainly coming from prompt muons, decay muons, hadronic punch-through, neutrons and muon induced electromagnetic secondaries. To achieve a good acceptance for such kind of events, the geometrical and kinematic acceptance for leptons has to be maximized. The significance of the signal will depend on the four lepton mass resolution. Hense a good lepton energy and momentum resolution at the level of 1% is necessary. For large Higgs boson masses the Higgs width increases rapidly and the signal will be rate limited, hence the accelerator luminosity becomes more important than the detector performance.

- Heavy Mass Higgs Boson ($M_H > 800GeV/c^2$):

  For a heavy Higgs boson the channel

$$H \rightarrow ZZ^{(*)} \rightarrow l^+l^-\nu\tilde{\nu} \tag{3-1-18}$$

becomes six times more frequent than $H \rightarrow ZZ^{(*)} \rightarrow l^+l^-l^+l^-$ and can be detected with the measurements of two high-p_T leptons and a high missing E_T due to the escaping neutrinos.

Also the channels

$$H \rightarrow WW, ZZ \rightarrow l^{\pm} + \nu + 2\,jets, 2l^{\pm} + 2\,jets \tag{3-1-19}$$

provide promising signatures for a heavy Higgs boson.

If these expectations are combined with a simulation of the detector response of the ATLAS experiment, it becomes possible to estimate how well the experiment will be able to find the Higgs boson. Figure 3.6 shows the sensitivity for the discovery of the Standard Model Higgs boson for several Higgs decay channels for the ATLAS experoment. The result shown here assumes an integrated luminosity decay channels for the ATLAS experiment. The result shown here assume an integrated luminosity of 100 fb^{-1}. The figure shows that if the Higgs boson exists, the ATLAS experiment will be able to observe it with a 5σ statistical significance over the full mass range from 100GeV/c^2 up to 1TeV/c^2.

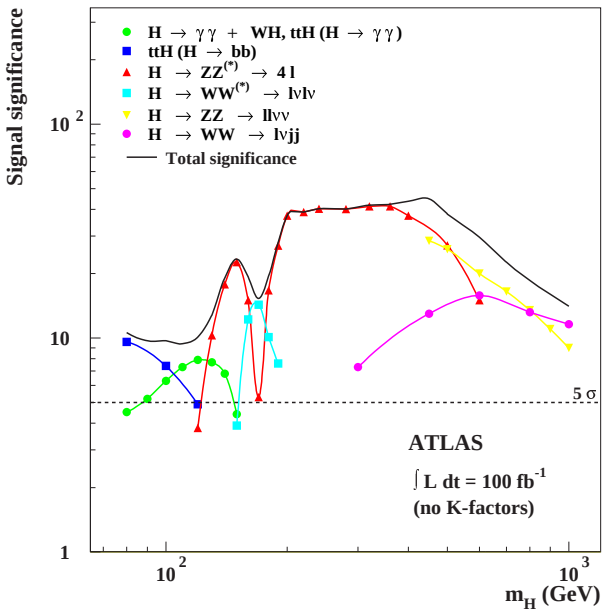

Figure 3.6: Decay width of the Higgs boson as a function of the Higgs mass

Chapter 4

The ATLAS

The ATLAS [9] is multi purpose detector installed in a LHC collision point. The ATLAS is characterized by its magnet configuration; a superconducting solenoid is installed around the Inner Detector and large superconducting air-core toroids consisting of independent coil is arranged with an eight fold symmetry outside the calorimeters. ATLAS is 22m in height and 44m in length and its weight is about 7,000 tons. Figure 4.1 shows a 3D view of the whole ATLAS detector.

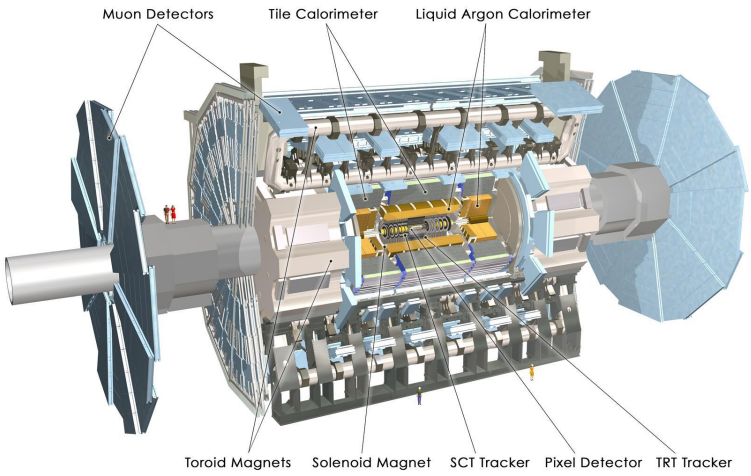

Figure 4.1: ATLAS Detector

For physics studies at the LHC, we need to know what kinds of particles are produced, by using combinations of various detectors. Behavior of particles in each detector is instructed in Figure 4.2. The produced particles can be distinguished by their differences of interaction with matters. For example, charged particles can be detected by a tracking detector and, by generating a magnetic

field and detecting their trajectories there, their momenta can be measured. Particles with electric charge and photons can be detected by an electromagnetic calorimeter and electrons and photons can be identified there. Strongly interacting particles such as mesons and nucleons can be detected by a hadron calorimeter. Since muons deposit little energy in the calorimeters and have a long life time, they reach outside of the calorimeters and are detected by the muon spectrometer. Details of each detector are explained later.

For not only particle identification but also event selection, combined information from the detectors is utilized. For example, b quarks and c quarks can be detected by following way. While t quarks immediately decay after its production, b hadrons and c hadrons have comparatively long life time and fly for a moment. Then they decay enough far away from the primary vertex and made the secondary vertices,. Therefore, b and c hadrons can be detected by finding the secondary vertices.

To exploit the full physics potential of the LHC, the ATLAS detector was designed to fulfill the following requirements;

- large acceptance and max η coverage for hermetic jet and missing E_T calorimetry.
- very good electoromagnetic calorimetry for electron and photon measurement.
- very good tracking efficiency for lepton momentum measurements, secondary vertex findings, and enhancement of the accuracy of electron and photon identification. Here tracking in jets have to be done;
- standalone muon momentum measurement at high luminosity.
- very low-p$_T$ trigger and reconstruction capability at low luminosity.

4.1 Definition of Coordinates

The coordinates in the ATLAS detector are defined as following. The beam line is defined as z-axis whose positive direction points in the direction of the LHC-b experiment. The plane transverse to the z-axis is defined as x-y plane. The positive x-axis is pointing from the interaction point to the center of the LHC ring and the positive y-axis is pointing to upwards.

While the Cartesian coordinate system is defined, basically cylindrical coordinates are used because of the detectors being cylindrically symmetric. In this case, the z-axis is the same as for the

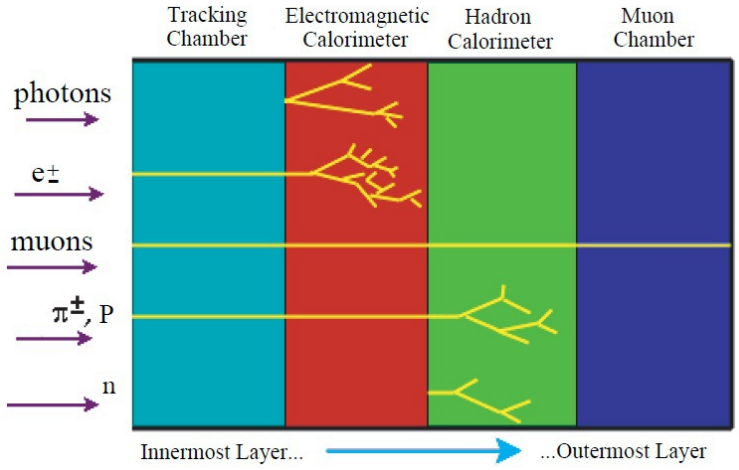

Figure 4.2: Behavior of PArticles in each Detector

Cartesian coordinate system. The azimuthal angle ϕ is defined as the angle from positive x-axis in x-y plane with the $-\pi$ to $+\pi$ range. The polar angle θ is also defined as the angle from the positive z-axis, and the psudorapidity as $\eta = -ln(tan\frac{\theta}{2})$. For hadron collider, η is often used because the particle distribution in pseudorapidity $\frac{\delta N}{\delta \eta}$ is basically flat.

4.2 DAQ System

The ATLAS trigger and data acquisition (DAQ) system is based on three levels of online event selection. Each trigger level refines the decisions made at the previous level and, where necessary, applies additional selection criteria. Starting from initial bunch crossing rate of 40.08 MHz (interaction rate of about 10^9 Hz at a luminosity of 10^{34}), the rate of selected events must be reduced to about 200 Hz for permanent storage. While this requires an overall rejection factor of 10^7 against so called minimum bias events, very good efficiencies must be retained for the rare new physics processes, such as Higgs boson decays.

4.2.1 Overview of the Trigger System

Figure 4.3 shows a simplified functional view of the Trigger and DAQ system. In the following, a brief description is given for some of the key aspects in the event selection process.

The first step of trigger system is named level-1(LVL1) trigger [21] which makes an initial se-

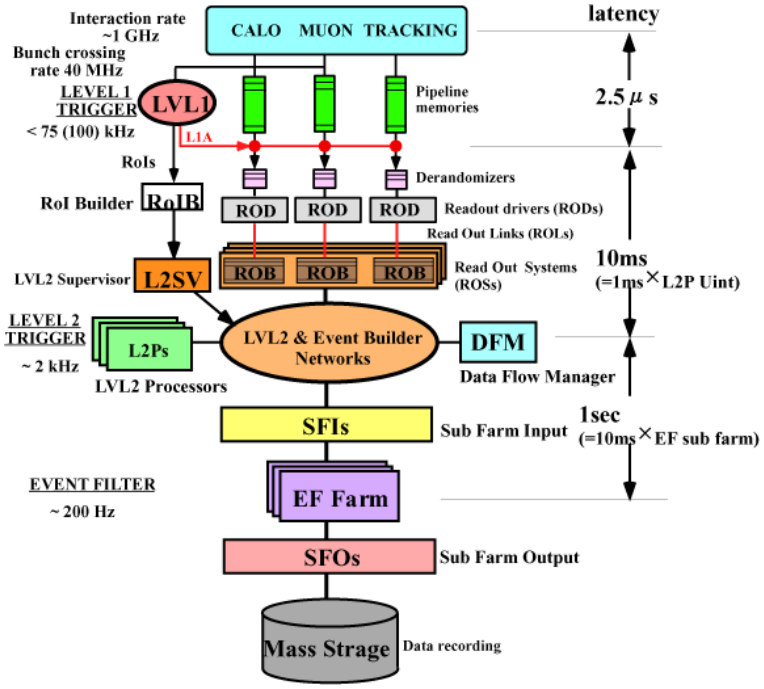

Figure 4.3: Block Diagram of the Trigger and DAQ for ATLAS

lection based on reduced granularity information from a subset of detectors. It consists of the muon trigger and the calorimeter trigger. In the muon trigger, high transverse momentum (p_T) muons are indentified using only the trigger chambers, RPCs (Resistive Plate Chambers) in the barrel and TGCs (Thin Gap Chambers) [23] in the endcap regions. Detailed description of the LVL1 muon trigger is in the next chapter of these trigger chambers and Muon Spectrometer. The calorimeter selections are based on reduced granularity information from all the calorimeters (EM and hadronic; barrel, endcap, and forward). Objects searched for by the calorimeter trigger are high-p_T electrons, photons, jets, and τ leptons decaying into hadrons, as well as large missing and total transverse energies. In the case of the electron/photon and hadron/τ triggers, energy isolation cuts can be applied. Trigger information is provided for a number of sets of p_T thresholds. The missing and total scaler transverse energies used in the LVL1 trigger are calculated by summing over the trigger towers. In addition, a trigger on the scaler sum of jet transverse energies is also available.

The LVL1 trigger decision is based on combinations of objects required in coinsidence or veto. Most of the physics requirements of ATLAS can be met by using, at the LVL1 trigger level, fairly simple selection criteria of a rather inclusive nature. However, the trigger implementation is flexible and it can be programmed to select events using more complicated signatures. The maximum rate

at which the ATLAS Front End system accepts the LVL1 trigger is limited to 75kHz in total. The rates are expected to be less than this limit but, in case, rates could be significantly reduced without major consequences for the physics programs, for example by increasing the thresholds on some of the inclusive (single object) triggers when operating at the highest luminosities and by relying more heavily on multi object triggers.

An essential requirement on the LVL1 trigger is that it should uniquely identify the bunch crossing of interest. Given the short bunch crossing interval(25ns), this is a non trivial consideration. It is important to keep the LVL1 latency (time taken to form and distribute the LVL1 trigger decision) to a minimum. During this time, information for all detector channels has to be conserved in "pipeline" memories. These memories are generally contained in custom integrated circuits, placed on or nearby the detectors. The LVL1 latency is required to be less than 2.5 μs.

All the detector data for the bunch crossing selected by the LVL1 trigger are held in the readout buffers, either until the event is rejected by the LVL2 trigger [22], in which case the data are discarded, or, in case the event is accepted by LVL2, until the data have been successfully transferred by the DAQ system to storage associated with the Event Filter [22], which makes the third level of event selection.

The LVL2 trigger makes use of Region of Interest(ROI) information provided by the LVL1 trigger. This includes information on the position η, ϕ, and p_T of candidate objects, and energy sums. The ROI data are sent from LVL1 to LVL2 for all events selected by the LVL1 trigger. Using the ROI information, the LVL2 trigger selectively access data from the readout buffers, moving only the data required to make the LVL2 decision. It is expected that LVL2 will reduce the rate less than 3.5kHz and latency of the LVL2 trigger is variable from event to event and is expected to be 40ms on average.

After LVL2, the last stage of the online selection is performed by the Event Filter. It employs offline algorithms and methods, adapted to the online environment, and use the most up to data calibration alignment information and the magnetic field map. The Event Filter will make the final selection of physics events written to mass storage for subsequent full offline analysis. The output rate from LVL2 should then be reduced by an order of magnitude, giving less than 200Hz, corresponding to an output data rate less than 300MB/s if the full event data are to be recorded.

4.3 Inner Detector

ATLAS Inner Detector is contained within a cylinder of length of 7m and a radius of 1.15m, in a solenoidal magnetic field of 2T. Momentum and vertex measurements are achieved with a combination of discrete high-resolution semiconductor pixel and strip detectors in the inner part of the tracking volume. Electron identification is performed by continuous straw tube tracking detectors with transition radiation capability in the outer part. Overall inner detector lay out is shown in Figure 4.4 and details for each detectors are mentioned below.

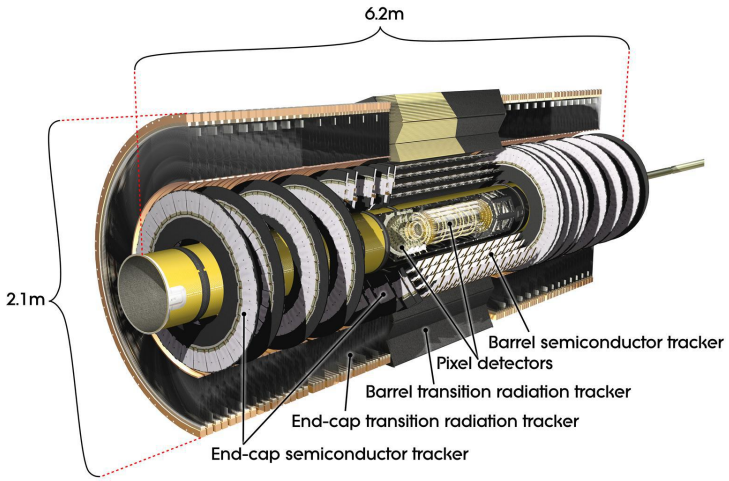

Figure 4.4: 3D overall inner detector layout

4.3.1 Silicon pixel vertex detector (PIXEL)

ATLAS Pixel detector provides a very high granularity and high precision set of measurements as close to the interaction point as possible. A Pixel sensor is a 16.4×60.8 mm wafer of silicon with 46,080 pixels, $50 \times 400 \mu$m each. Each sensor is readout by 16 chips, each serving an array of 18 by 160 pixels. The 80 million pixels cover an area of 1.7 m^2. The system consists of three barrels at average radii of about 5, 9 and 12 cm (1456 modules) respectivly, and three discs on each side between radii of 9 and 15 cm (288 modules), as shown in Figure 4.5. The modules are overlapped on the support structure to give hermetic coverage. The thickness of each layer is expected to be about 2.5 % of a radiation length at normal incidence. Typically three pixel layers are crossed by each track.

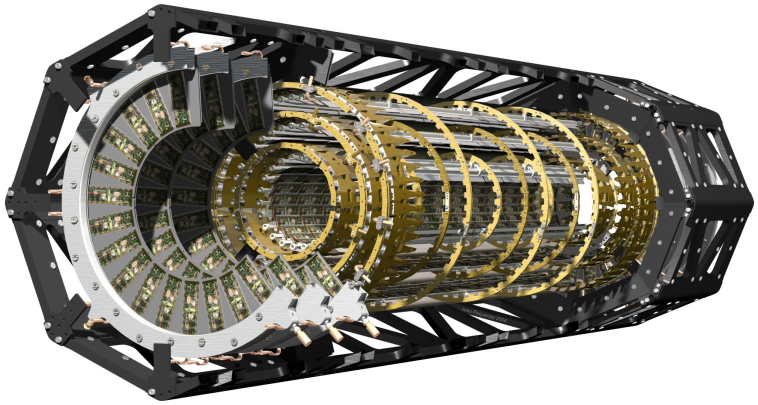

Figure 4.5: Pixel Detectors

4.3.2 Semi Conductor Tracker (SCT)

The SCT system is designed to provide four precision measurements per track in the intermediate radial range, contributing to the measurement of momentum, impact parameter and vertex position, as well as providing good pattern recognition by the use of high granularity. The system is an order of magnitude larger in surface area than previous generations of silicon microstrip detectors, and in addition, must face radiation levels which will alter the fundamental characteristics of the silicon wares themselves.

Figure 4.6 shows 3D view of the SCT system, which covers $|\eta|$ <2.5. The barrel SCT uses four layers of silicon microstrip detectors to provide precision points in the r-ϕ and z coordinates. Each silicon detector is $6.36 \times 6.40 cm^2$ with 768 readout strips each with 80 μm pitch. Each modul consists of four detectors. On each side of the module, two detectors are wire bounded togetger to form 12.8 cm long strips. Two such detector pairs are then glued together back to back at a 40mrad angle, separated by a heat transport plate, and the electronics is mounted above the detectors on a so-called hybrid. The readout chain consists of a front end amplifier and discriminator, followed by a binary pipeline which stores the hits above threshold until the arrival of the first level trigger decision. The forward modules are very similar in construction but use tapered strips, with one set aligned radially. Forward modules are made with either about 12 or 7 cm lengths. The detector contains 61 cm^2 of silicon detectors with 6.2 million readout channels. The spatial resolution is 16 μm in r-ϕ and 580 μm in z. Tracks can be distinguished if separated by more than about 200 μm.

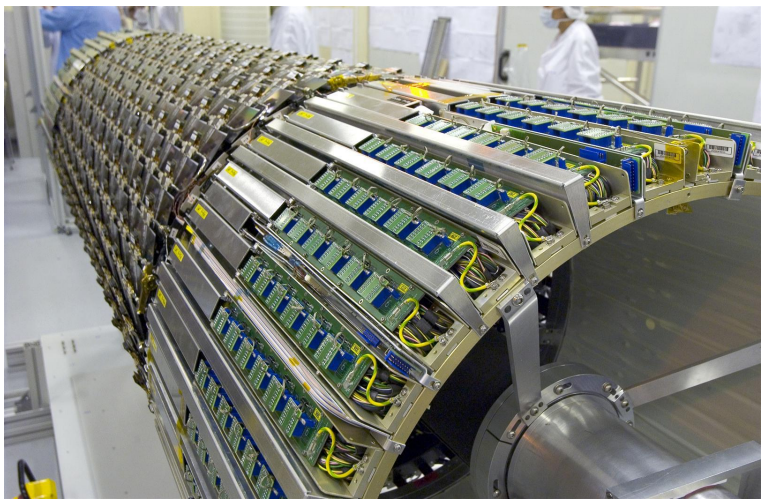

Figure 4.6: SCT

4.3.3 Transition Radiation Tracker (TRT)

TRT is based on the use of straw detectors, or tubes, which can operate at the expected high rates due to their small diameter and the isolation of the sensitive wires within individual gas volumes. Electron identification capability is added by employing Xenon gas to detect transition radiation photons created in a radiator between the straws. The nonflammable gas mixture is Xe:CO_2:O_2 = 70:27:3 with a total volume. The barrel section is built of individual modules covering the radial range from 56 cm to 107 cm. Each endcap consists of 18 wheels. Each channel provides a drift time measurement that gives a spatial resolution of 170 μm per straw.

4.4 Calorimeters

In contrast to the inner detectors, such as magnetic spectrometers, intrinsic resolution of calorimeters[19] improves with energy, which makes themselves very suitable detectors at high-energy machines.

The task of the calorimeters at hadron colliders are the followings;

- Accurate measurement of the energy and position of electrons and photons.
- Measurement of the energy and direction of jets and measurement of the missing transverse energy (E_T) of the event.
- Particle identification, for instance separation of electrons and photons from hadrons and jets,

and tau hadronic decay from jets.

- Event selection at the trigger level.

The overall detector layout is shown in Figure 4.7. Highly granular Liquid Argon (LAr) electromagnetic sampling calorimeter [18], with an emphasis on energy and position resolution, covers the pseudorapidity range $|\eta|$ <3.2. At large rapidities, higher radiation resistance is needed and the intrinsically hard LAr technology is used. In the endcap, the LAr technology is also used for the hadronic calorimeters. There are special LAr forward calorimeters which extend the pseudorapidity coverage to $|\eta| = 4.9$. The LAr calorimetery is contained in a cylinder with an outer radius of 2.25m and extends longitudinally to $\pm 6.75m$ along the beam axis. The bulk of the hadronic calorimetry is provided by scintillator tile calorimeters, which is separated into a large barrel and two smaller extended barrel cylinders are 4.25m and its half length is 6.10 m. The overall calorimeter system provides good jet and missing E_T performance of the detector.

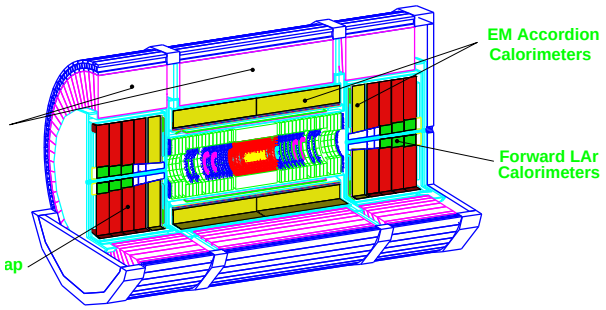

Figure 4.7: overall Calorimeter Layout

4.5 Muon Spectrometer

Muons interact weakly and electromagnetically like electrons, but they can reach outside of the calorimeters because muon mass is almost about 200 times heavier than electron mass. Therefore, the muon spectrometer is placed at the outermost of the detectors.

High momentum final state muons are one of the most promising and robust signatures of physics at the LHC. To exploit this potential, the ATLAS is equipped with a high resolution muon spectrometer [16] with stadalone trigger and momentum measurement capability over a wide range of transverse momentum(p_T), pseudorapdity(η), and azimuthal angle(ϕ). Muon measurement at ATLAS is based on the magnetic deflection measurement of muon tracks in a system of the large superconducting air

core toroids instrumented with tracking chambers. Four type of muon spectrometers are installed in ATLAS detector, two of them, Resistive Plate Chamber and Thin Gap Chambers are trigger chambers and the other, Monitored Drift Tube and Cathode Strip Chamber are for precision measurement. In the range $|\eta|$¡1.0, bending fields are provided by a large barrel magnet consisting of eight coils surrounding the hadron calorimeter. For $1.4 < |\eta| < 2.7$, muon tracks are bent in two smaller endcap magnets inserted into both end of the barrel toroid. In the interval $1.0 < |\eta| < 1.4$ magnetic deflection is provided by a combination of barrel and endcap fields. This magnet configuration provides a field that is mostly orthogonal to the muon trajectories, while minimizing the degradation of resolution due to multiple scattering.

The detailed description about each muon spectrometer is mentioned in chapter 5 of ”Muon Spectrometer”.

Chapter 5

Muon Spectrometer

ATLAS is a multi purpose detector for LHC and consists of several detector parts. Muon detectors [16] are a part of ATLAS and play following two roles; momentum measurements with precise chambers and event trigger for muons with trigger chambers.

A quarter view of the Muon system in R-Z plane is shown in Figure 5.1.

In both the barrel and endcap region, there are 3 stations of muon chambers.

There are 3 air-core toroidal magnets; a barrel magnet with 26 m long and 19.5m in radius, and two endcap magnets with 5.6 m long and 3 m in radius. The pictures of these magnet are shown in Figure 5.2 and 5.3. Trajectories of a muon from the interaction points are bent in these toroidal magnetic fields. Momentum of the muon can be obtained by measurement of the curvature of the track.

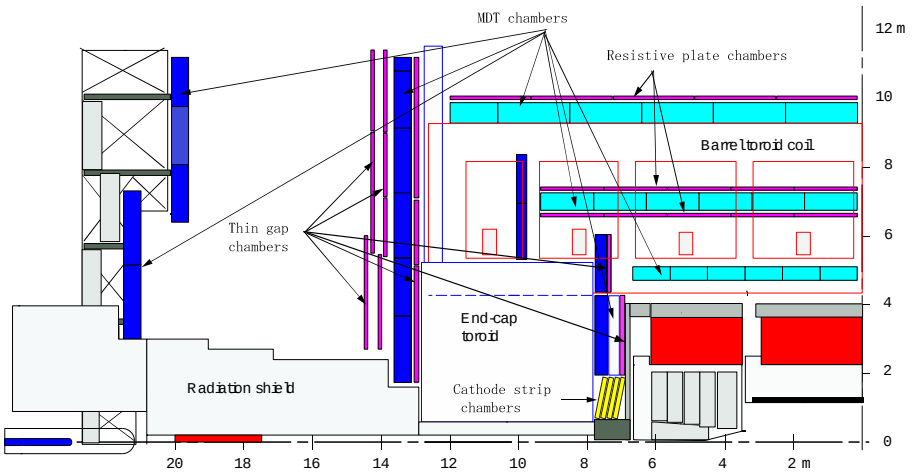

Figure 5.1: R-Z View of the ATLAS Muon System

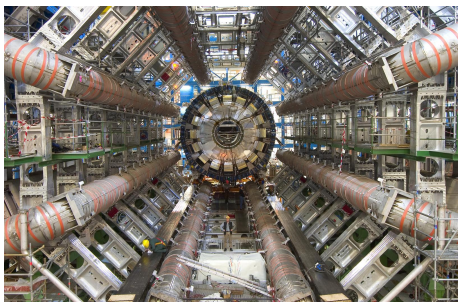

Figure 5.2: Barrel Toroid Magnet

Figure 5.3: Endcap Toroid Magnet

5.0.1 Measurement Method of Muon

A popular method about measurement of muon track is to focus to transverse momentum measurement.

The momenta of charged particles can be calculated by detecting their trajectories in the magnetic field. If a track is detected at three equally spaced points, the sagitta s of an indication of bentness is defined as shown in Figure 5.4 and can be calculated as

$$s = R(1 - cos\frac{\alpha}{2}) \sim \frac{R\alpha^2}{8} \tag{5-0-1}$$

Then the momentum P of a charged particle in magnetic field B is calcurated as

$$P = 0.3BR \tag{5-0-2}$$

whre R is the measured radius of the orbit, then concerning α to be

$$\alpha = 0.3\frac{BL}{P} \tag{5-0-3}$$

the sagitta is represented as

$$s = 0.3\frac{BL^2}{8P}. \tag{5-0-4}$$

Thus, the momentum can be obtained from measurement of sagitta.

Measurement of sagitta is a basical algorithm for measurement of p_T, to find and select high p_T muon track.

LVL1 Muon System measures sagitta of muon candidates using several layers of detectors. In nominal case, high p_T muon may have small sagitta. But ATLAS magnetic field is not uniform and even in some region that as almost no integrated magnetic field. It affects bentness of muon tracks dependents on their location of tracks.

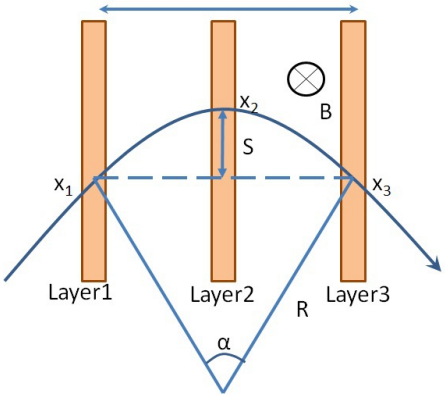

Figure 5.4: Measurement of Sagitta

5.1 Precision Chamber

Two types of precision chambers are installed in ATLAS muon spectrometers. They are Monitord Drift Tube (MDT) and Cathode Strip Chamber (CSC).

MDTs are installed in barrel region and endcap region, and cover $|\eta| < 2.0$, CSCs are installed in forward region and cover $2.0 < |\eta| < 2.7$.

Precision chambers measure the track coordinates in bending direction with high precision.

5.1.1 Monitored Drift Tube

The Monitored Drift Tube (MDT) measures position of charged tracks precisely in the bending direction of the toroidal magnet. The basic element of MDT is an aluminium drift tube. Its diameter

Parameter	Value
Tube Material	Al
Outer Tube Diameter	29.970mm
Tube Wall Thickness	0.4mm
Wire Material	gold-plated W/Re (97/3)
Wire Diameter	50 μm
Gas Mixture	Ar:CO_2 = 97:3
Gas Pressure	3.0 bar
Gas Gain	2×10^4
Applied Voltage	$3080V$
Maximum Drift Time	about 700ns
Average Resolution per Tube	80 μm

Table 5.1: MDT Parameters

is 29.970mm, with the wall thickness of 0.4mm. A Tungsten-Rhenium wire of diameter 50 μm is strung at the center of tube. The wire is fixed on the cylindrical end plug which keeps the spacial position of wire with respect to the tube with good accuracy. The tube is filled with Ar(97):CO2(3) gas at 3 bar. Applied High Voltage for the wire with average gain of 2×10^4.

The maximum drift time is about 700ns and average of spacial resolution per tube is about 80 μm. The main parameters of the MDT are summarized in Table 5.1.

MDT tubes are packed together and form a chamber. MDT is installed in three stations; inner, middle and outer. Middle and outer MDT stations consist of three layers and inner MDT station consists of four layers.

The position and deformation affect momentum quality of MDT. They should be known to a precision of 30 μm. An optiacal monitoring sensor to align the MDT form a laser-based alignment system which consists of three active elements of LED, lens and CCD camera. The resolution of measurement is about 1 μm.

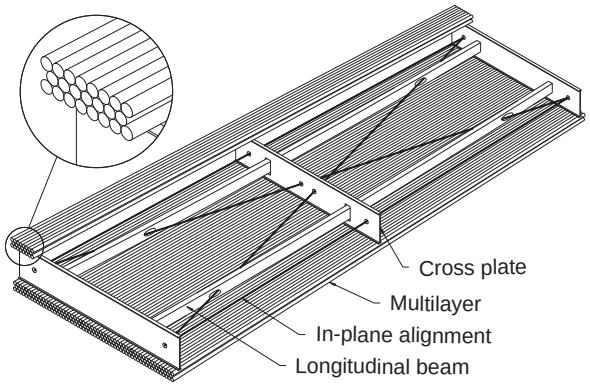

Figure 5.5: A Schematic View of MDT for Barrel

5.1.2 Cathode Strip Chamber

CSC is Multi Wire Proportional Chambers(MWPC) with a cathode strip readout. Position resolution of charged tracks is 60μm.

The MDT can not be operated in the forward region where high counting rate (>200KHz/cm2) is expected, because the drift time of MDT is rather long

CSCs are installed in high counting rate area, and covers upto $|\eta| < 2.7$. The capacity of counting rate for CSC is 1kHz/cm^2 was expected. The schematics of CSC is shown in Figure5.6. Anode wire diameter is 30μm. Applied high voltage is 1900V. The gain achieves 6×10^6 Electron drift time should be less than 40ns resulting a time resolution of 7ns. Applied gas is composed of Ar/CO_2 = 8:2. It has low neutron sensitivity (less than 10^{-4}).

Two types of CSCs are installed; small chamber and large chamber. Readout strip pitch is 5.31mm for large chamber, and 5.56mm for small chamber. Track coordinate resolution of CSC is achieved 60 μm, ant the resolution of ϕ direction is about 5mm.

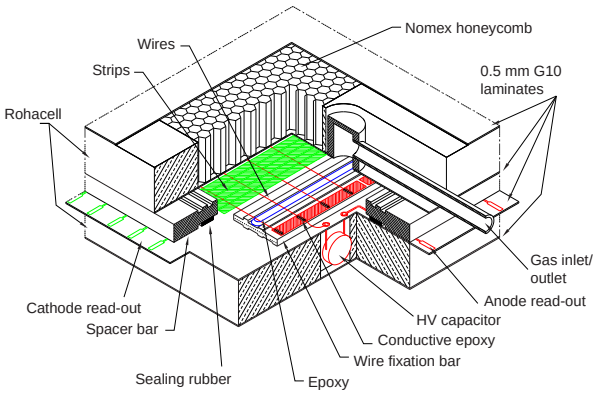

Figure 5.6: Cathode Strip Chamber

5.2 Trigger Chamber

ATLAS DAQ has trigger system to reduce background and choose the interesting phenomena among huge background events. LVL1 Muon Trigger is a part of first stage of ATLAS trigger system. The LVL1 trigger, which optimized to find high p_T muons is implemented in ATLAS trigger system.

The main role of the Trigger Chambers is find and select the most interesting high p_T muon in each bunch crossing and provide L1A (Level1 Accept) in each detector system.

Two types of trigger chambers are installed in ATLAS muon system. They are Resistive Plate Chamber (RPC) and Thin Gap Chamber (TGC). Six layers of RPCs are installed in barrel region which covers $|\eta| < 1.05$. Seven layers of TGCs are installed in Endcap regions which cover $1.05 < |\eta| < 2.4$ on both sides. Both chambers generate fast signal, whose response time achieves in order of nano seconds. Position resolution is required to be about 1cm; it is enough to do coarse p_T measurement and track identification. Second coordinate measurement about 5cm is required because MDT has few sensitivity for ϕ direction, for higher level trigger and offline analysis.

5.2.1 Resistive Plate Chamber

The Resistive Plate Chamber is a gaseous detector. It does not have any wires. Two parallel plates are faced with a gap of 2mm. The plates are made of 2mm thick of Bakelight with resistive surface. (volume resistivity is 1 to $5 \times 10^{10}\Omega$)

9.8 kV of applied voltage allows avalanches along charged tracks with a streamer probability of less than 1%. Readout metal plate is put on the outer faces of resistive plates. The filled gas

is $C_2H_2O_4(94\%)/Iso - C_4H_{10}(5.0\%)/SF_6(0.3\%)$. The position resolution in η coordinate and ϕ coordinate is about 10mm and time resolution achieved less than 10ns. The local rate capability is about 1kHz/cm^2.

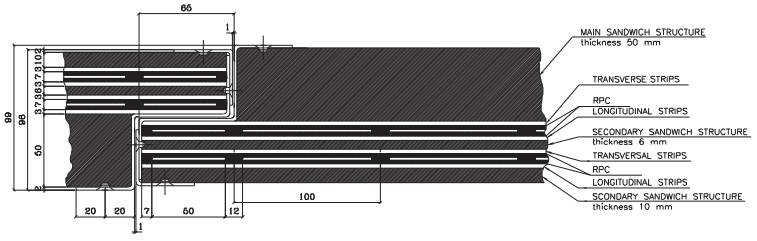

Figure 5.7: Resistive Plate Chamber

5.2.2 Thin Gap Chamber

Thin Gap Chamber(TGC) is a trigger chamber and installed in both endcap region, and TGCs are installed like a wheel structure(Figure 5.8). The small η region is named Endcap and covers $1.05 < |\eta| < 1.9$ for each side, and the large $|\eta|$ region named Forward and covers $1.9 < |\eta| < 2.4$.

TGC has two types channel readout of anode wire and cathode strip. The diameter of anode wire of tangsten with Au coating is 50 μm. The distance between wire anode and strip cathode are shorter than the distance between wires as shown in Figure 5.9. The cathode consists of carbon coated glass-epoxy which surface resistance is 1M$\Omega/\square$. This thin gaps make shorter drift time and high time resolution. Two graphite cathode plane on FR4 board are placed 1.4 mm from the wire plane. The pick up strip of copper on the outer surface of FR4 are formed in orthogonal direction to the wire, this structure makes two dimensional position information. To keep the gap between anode and cathode, wire supports are placed as shown in the Figure 5.11.

The optimized HV is applied for each chamber. The volumes are determined taking into account number of noisy channel, and hit efficiency. Applied voltage is 2800V is default, but higher voltage upto 2950 V is applied for low gain chambers.

Two types of TGC are fabricated; doublet type and triplet type. Doublet TGC consists of 2 layers wire and 2 layers strip. Wire and strip pair sandwiches honeycombs. This honeycomb structure reinforces the strength of TGC with light weight. Triplet TGC consists of 3 layers wire and 2 layers of strip. There are three pairs of cathodes but only outer layers are picked up. Cross section of TGCs

are shown in Figure 5.10

Chambers are filled with gas of CO_2:n-pentane [17] = 55:45. This type of cell geometry allows operation in limited-propotional mode.

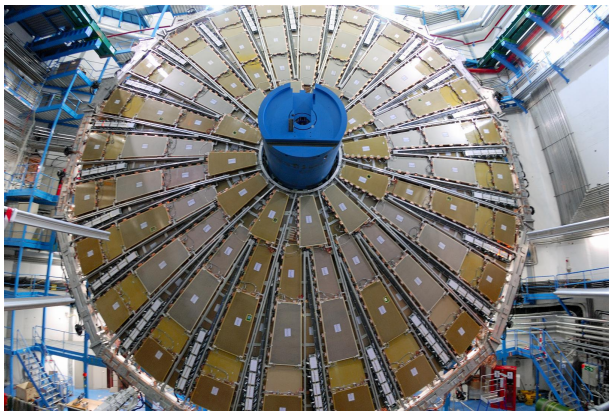

Figure 5.8: Installed TGC Big Wheel

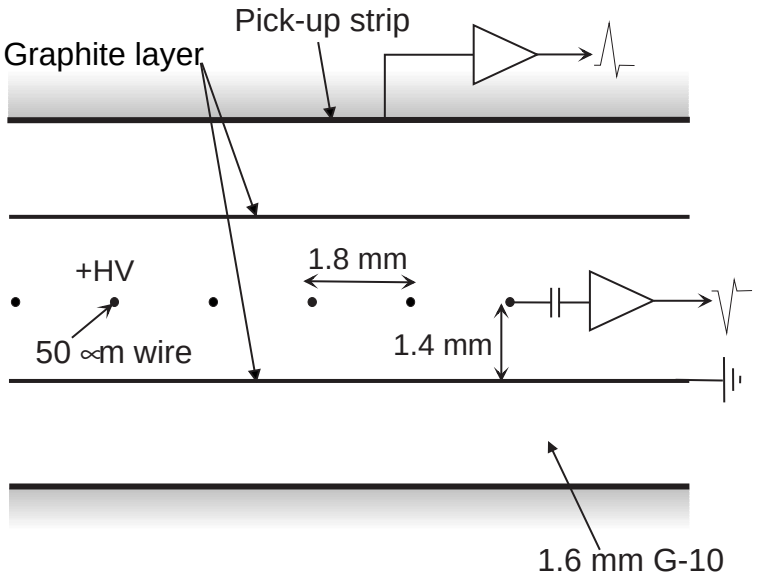

Figure 5.9: Structure of TGC

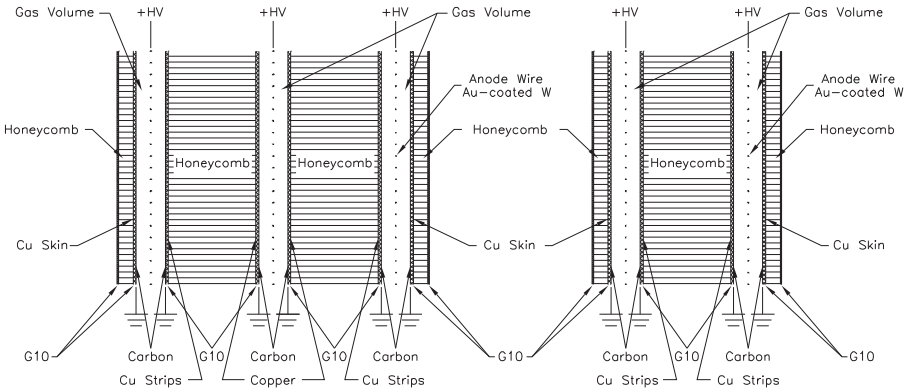

Figure 5.10: Cross section of triplet (left) and doublet (right) TGCs

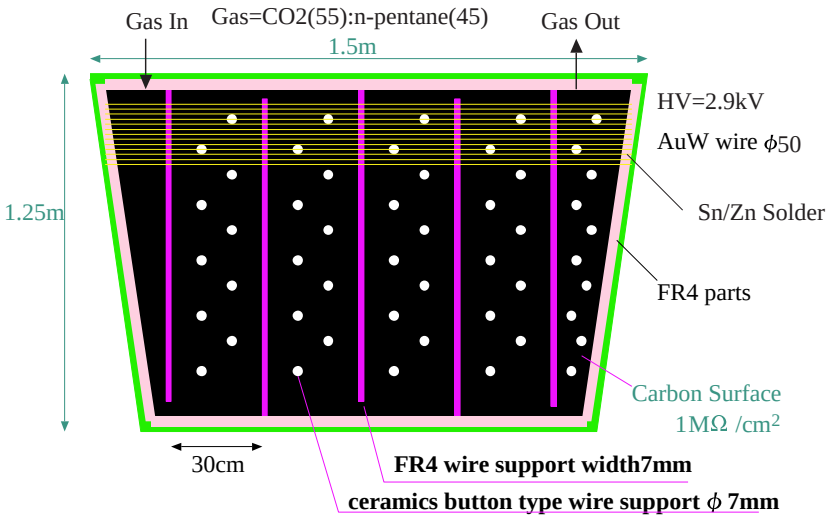

Figure 5.11: Structure of TGC Wire Support

5.3 Toroidal Magnet

Each toroidal magnet consists of eight flat coils as octant symmetrically around the beam axis, Endcap coils are interleaved between barrel coils.

Integrated intensity of magnetic field in barrel region is 2 to 6 Tm, and the one in endcap region is 4 to 8 Tm as shown in Figure 5.12.

Figure 5.13 shows line of magnetic field at Z=10m. In the interference region of barrel and endcap magnets (r=400~500cm), magnetic field is not uniform and not along ϕ direction.

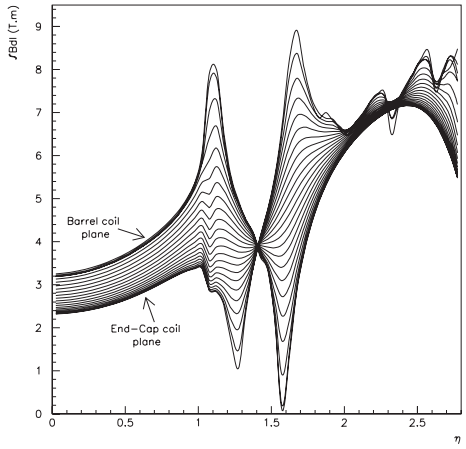

Figure 5.12: Magnetic Field Distribution in η. Horizontal axis means η, and vertical axis means the integrated intensity of magnetic field(Tm).

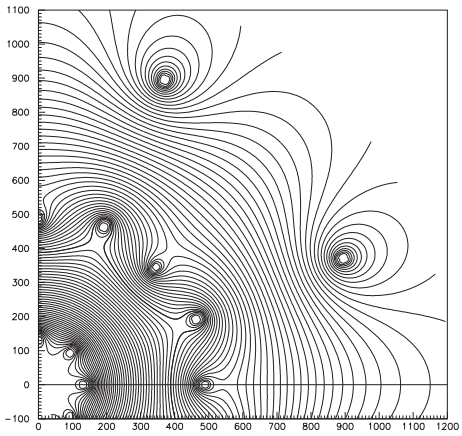

Figure 5.13: X-Y View of Magnetic Field at Z = 10m (Horizontal axis means X coordinate, and vertical axis means Y coordinate.)

5.4 LVL1 Muon Trigger

Muon system has a triggering step of LVL1 in the scheme of ATLAS DAQ. A schematic of the ATLAS LVL1 Muon Trigger is shown in Figure 5.14. LVL1 Muon Trigger is provided from barrel and endcap chambers. Muon candidates are selected in endcap and barrel region in parallel. MuCTPI combines these information and send it to the CTP.

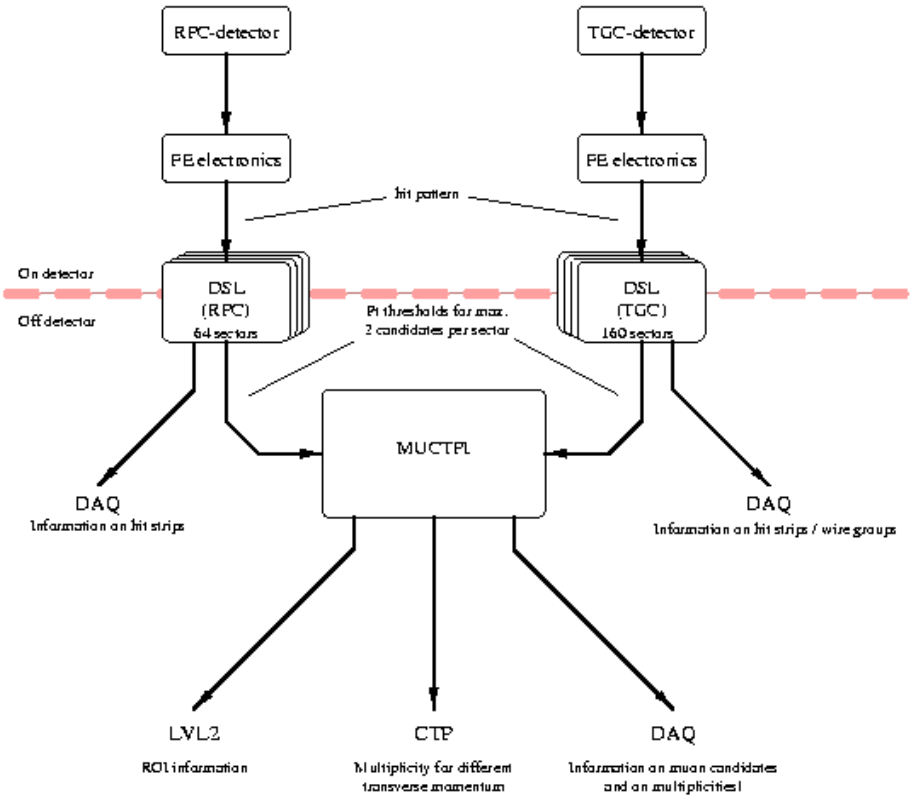

Figure 5.14: A Schematic of the ATLAS LVL1 Muon Trigger

5.4.1 Requirements of LVL1 Muon Trigger

The LVL1 Muon Trigger aims to find high p_T muons and reduce the trigger rate upto 15kHz at maximum.

Algorithm of LVL1 Muon Trigger is processed without deadtime, and it must be produced in each beam collision. The information of LVL1 Muon Trigger consists of position information of ROI, discriminated p_T in six level, and Bunch Crossing Identification (BCID).

5.4.2 Muon to Central Trigger Processor Interface (MuCTPI)

MuCTPI has a role to pass LVL1 Muon Trigger Candidates to CTP from RPC and TGC. Each LVL1 Muon Trigger provides the information of trigger candidate consisting of position information and six level of pT threshold information. MuCTPI receives these infomatin, and treat the chamber overlap and boundary.

Trigger information will be sent to CTP.

Chapter 6

Endcap Muon Trigger

TGC is used to provide the LVL1 Encdap Muon Trigger

LVL1 Endcap Muon Trigger is processed using dedicated electronics online. Processes in these electronics are in the pipeline provide the trigger of consecutive beam collisions.

Coincidence of TGC hits between three stations on each side gives good trigger efficiencies with enough p_T resolution and background rejections. In this chapter, how to achieve the ATLAS required performance will be presented from the viewpoints of algorithm, electronics, and implementation.

6.1 Overview of LVL1 Endcap Muon Trigger

LVL1 Endcap Muon Trigger system covers $1.05 < |\eta| < 2.4$ in both sides of ATLAS.

TGC chambers are installed in 4 stations; Inner, M1, M2, M3. M1, M2 and M3 stations are parts of the Big Wheel located at z of about 14m. In the M1 station, TGCs with three gas gaps (called Triplet type) are installed. TGCs with two gas gap (called Doublet type) are installed in other stations. Figure 6.1 shows a cross-section of TGC stations.

At first, hits on the pivot plane (TGC at M3) are used to draw the infinite momentum path for a muon candidate. A window for the coincidence is defined for each trigger plain (TGCs in M2 and M3) in R and ϕ directions around the infinite momentum track. Coincidenced signals of R-ϕ will make a trigger candidate if a hit is found in the window corresponding to the hit position in the pivot plane. The deviation from infinite momentum and observed hits found in trigger planes is related to the momentum. Overview of LVL1 Endcap Muon Trigger algorithm is shown in Figure 6.2.

The LVL1 Endcap Muon Trigger system consists of 3 parts of coincidence; 2 station coincidences, 3 station coincidences and R-ϕ coincidences, as shown in Figure 6.3. In 2 station coincidences and

3 station coincidences, R and ϕ information are processed in parallel. In 2 station coincidences, at least 3 hits are required among 4 layers at M2 and M3 (pivot) station. The 2 station coincidence is called Low-pT coincidence because it can cover lower p_T tracks. In 3 station coincidences, hits in M1 station are required in addition to 2 station coincidences. The 3-station coincidences is called High-pT coincidence. Track sagitta of δR and $\delta\phi$ are calculated in both 2 station coincidences and 3 station coincidences.

Final decision of LVL1 Endcap Muon Trigger is done by R-ϕ coincidences. It selects muon candidates and determines their Region of Interest (ROI), p_T level, and Bunch Counter ID(BCID). These information will be sent to Central Trigger Processor through Muon Central Trigger Processor.

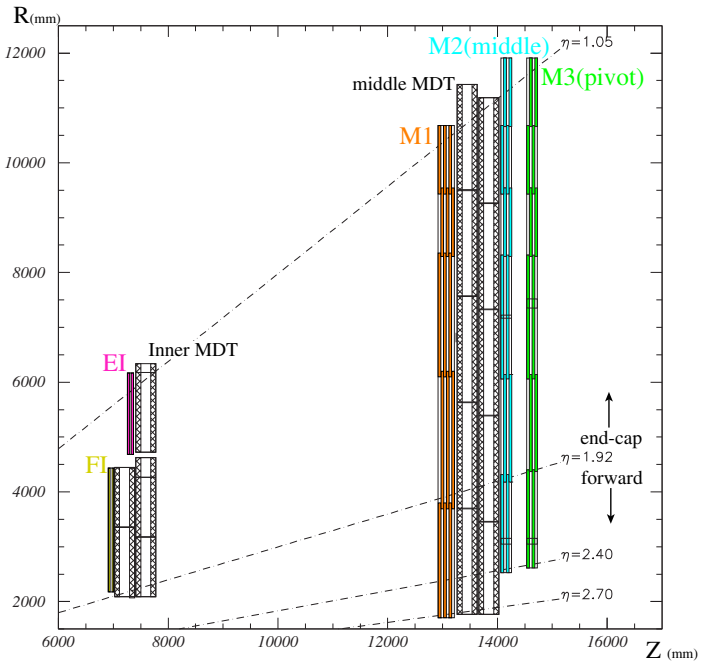

Figure 6.1: A cross-section of the TGC Stations. (Horizontal axis means z position(mm), and vertical axis means position of radius R(mm).)

6.1.1 Big Wheel

Three stations of TGCs, M1, M2 and M3, are called as Big Wheel. TGCs in the Big Wheel in each side cover $1.05 < \eta < 2.4$ and can be divided into two regions, Endcap and Forward; $1.05 < \eta < 1.9$ is Endcap region, and $1.9 < \eta < 2.4$ is Forward region.

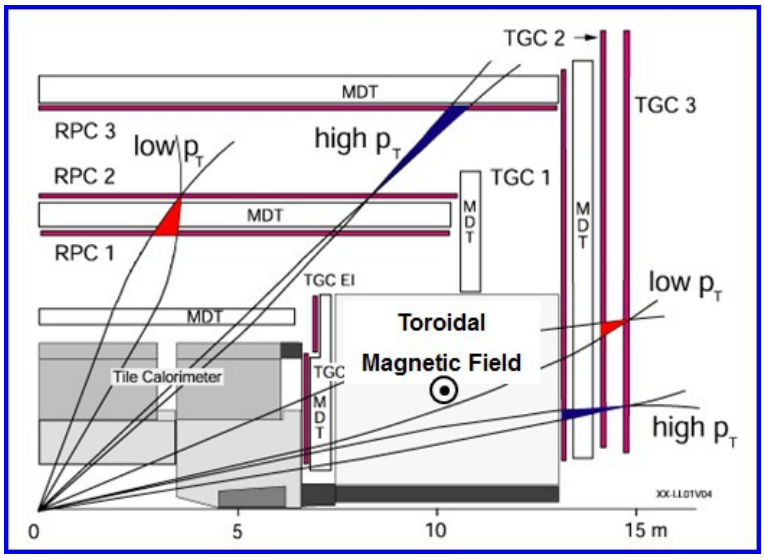

Figure 6.2: A cross-section of the of LVL1 Endcap Muon Trigger Scheme (Horizontal axis means z position(m), and vertical axis means radius.)

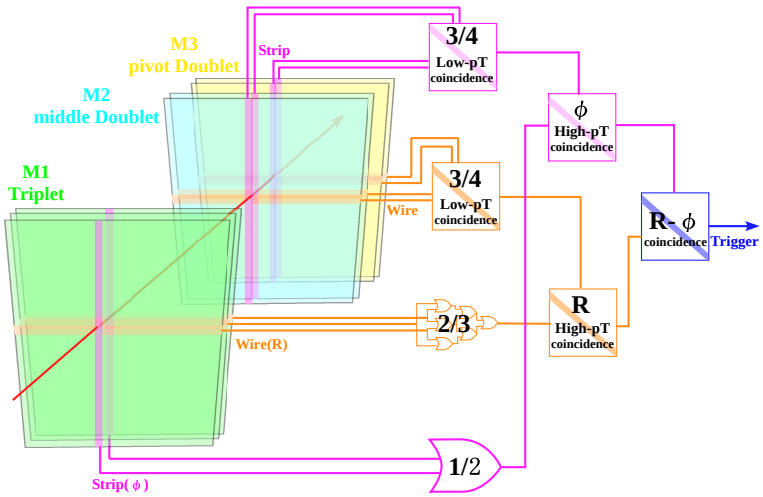

Figure 6.3: Coincidences between stations in LVL1 Endcap Muon Trigger

Pivot plane (M3 station) in Endcap region consists of 5 TGC chambers numbered from small $\eta(1)$ to large $\eta(5)$, and Forward region contains one TGC chamber, (as shown in Figure 6.4)

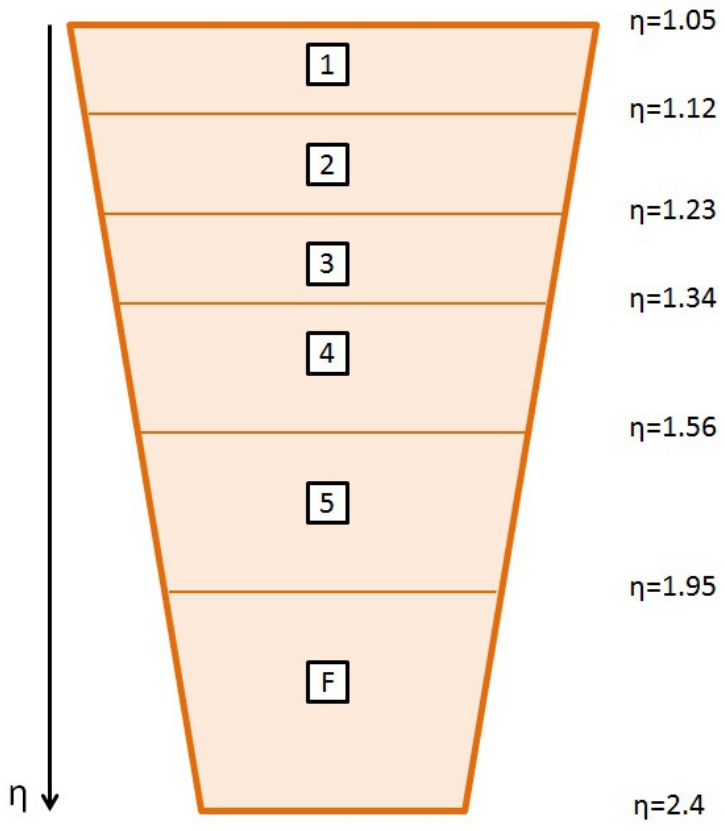

Figure 6.4: TGC numbering on pivot plane

Trigger Sector is defined for the operation and implementation of LVL1 Endcap Muon Trigger. Each trigger sector can provide upto 2 muon candidates in each bunch crossing. ROI is an unit for position of trigger information. Each muon candidates is sent to CTP with its ROI and p_T level. The Forward region contains 24 trigger sectors divided in ϕ direction. A trigger sector contains 64 ROIs, 16 divided in the R direction and 4 divided in the ϕ direction.

A Forward Trigger Sector is 24 divided for ϕ direction. ROI is defined as a region of 8 divided for the R direction and 4 divided for the ϕ direction.

6.1.2 Small Wheel

Small wheel is installed at about z = 7m and consists of Endcap Inner (EI) and Forward Inner (FI). EI and FI are Doublet TGCs. Small wheel covers $1.05 < |\eta| < 1.9$. FI covers all ϕ region, but EI has

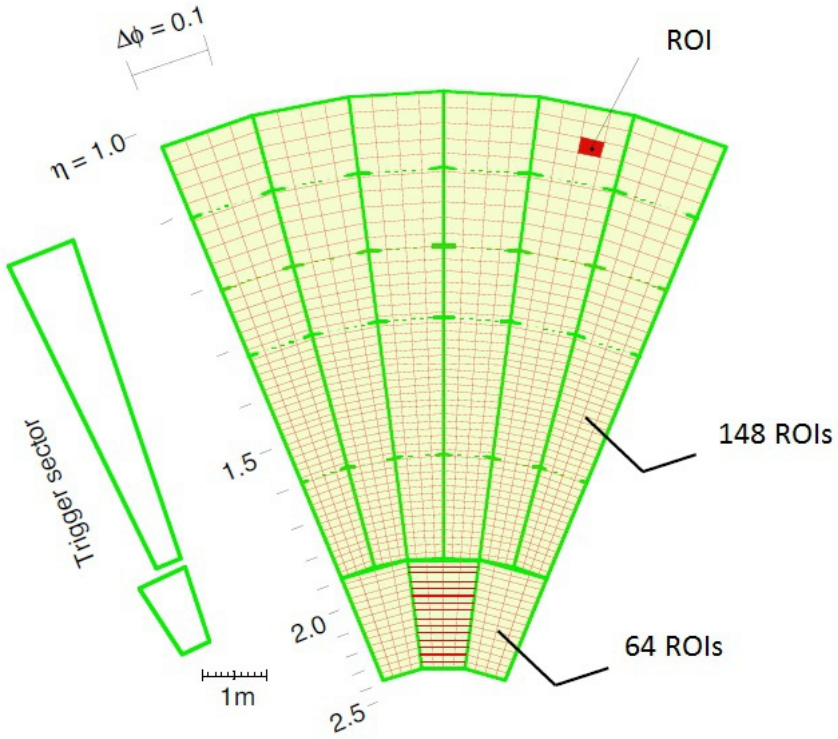

Figure 6.5: Trigger Sector and ROIs in the sector. Each region surrounded by green line corresponds to a trigger sector, and a red colored cell is an example of ROI.

21 sectors and 8 holes toroidal magnet coils as shown in Figure 6.6 and 6.7.

Hit information on Small Wheel are not used in the current scheme of LVL1 Endcap Muon Trigger, but they are used in higher level trigger(LVL2 and Event Filter).

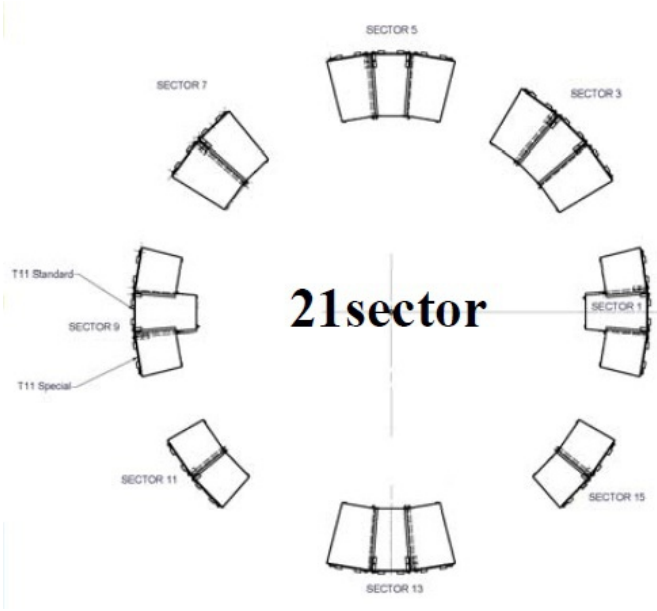

Figure 6.6: Overview of Endcap Inner

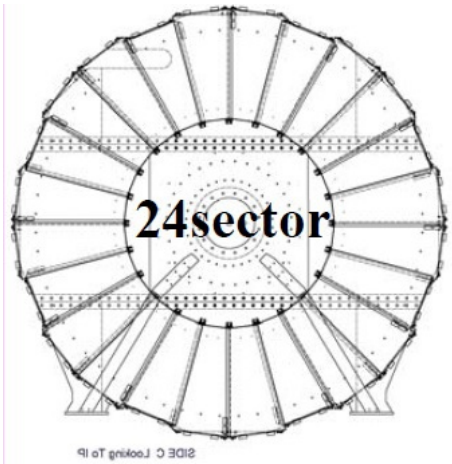

Figure 6.7: Overview of Forward Inner

6.2 Implementation on the TGC Electronics System

Detailed description on the Endcap muon trigger system is presented in this section.

Figure 6.8 shows an overview of the TGC electronics scheme. Both wire and strip signals are transmitted to Amplifier Shaper Discriminator (ASD) [25][26] circuits. Four circuits are impelemented in an ASD chip, and four ASD chips are mounted on an ASD board. So, each ASD board can handle 16 channels. ASD boards are installed on the edge of a TGC and enclosed inside the TGC electronics shielding.

Signals from ASD board are sent to PS-Boards. Patch-Panel (PP) ASICs, Jtag Routing Controller(JRC), embeded Local Monitor Board (eLMB) and Slave Board (SLB) ASICs [27] are mounted on the PS-Board. PS Boards are placed on surface of the TGC wheels. Electronics for doublets are mounted on the outer surface of M3 and those for the triplets on the inner surface of M1.

Hit information in an event will not reach at same time without timing adjustment PP ASICs. Hit information in each bunch is sent to SLB ASICs, where 2 station coincidence and readout circuits are placed. Trigger information (position and sagitta) from the 2 station coincidence is encoded and passed to High-pT coincidence(HPT) Boards [28]. HPT boards are installed in HSC crates placed near the outer rim of the M1 wheel. Signals from doublet and triplet SLBs are combined to find tracks in R-z plane and R-ϕ plane independently.

Trigger signals from both wire and strip HPT boards are sent the Sector Logic (SL) via optical link between the ATLAS detector and the counting room(USA15). The SL contains R-ϕ coincidence and track selector circuit to find muon candidates (upto 2 candidates in each trigger sector) with p_T and position information. Six level of p_T threshold will be determined in SL to select highest p_T candidate. Region of Interest (ROI) will be determined by wire and strip coincidence coordination for each candidate. These trigger candidates are sent to Muon Central Trigger Processor (MuCTPI). The SL has SLB ASICs also to read out information from HPT boards and trigger results. The detail of SL will be described in next chapter. Hereafter the electronics boards in each step and described in detail.

6.2.1 ASD

Each ASD board has 4 ASD chips and handles 16 channels of wire and strip signals from TGCs. ASD ASIC contains 4 channels of two-stage amplifiers with a base-line restorer and discriminators.

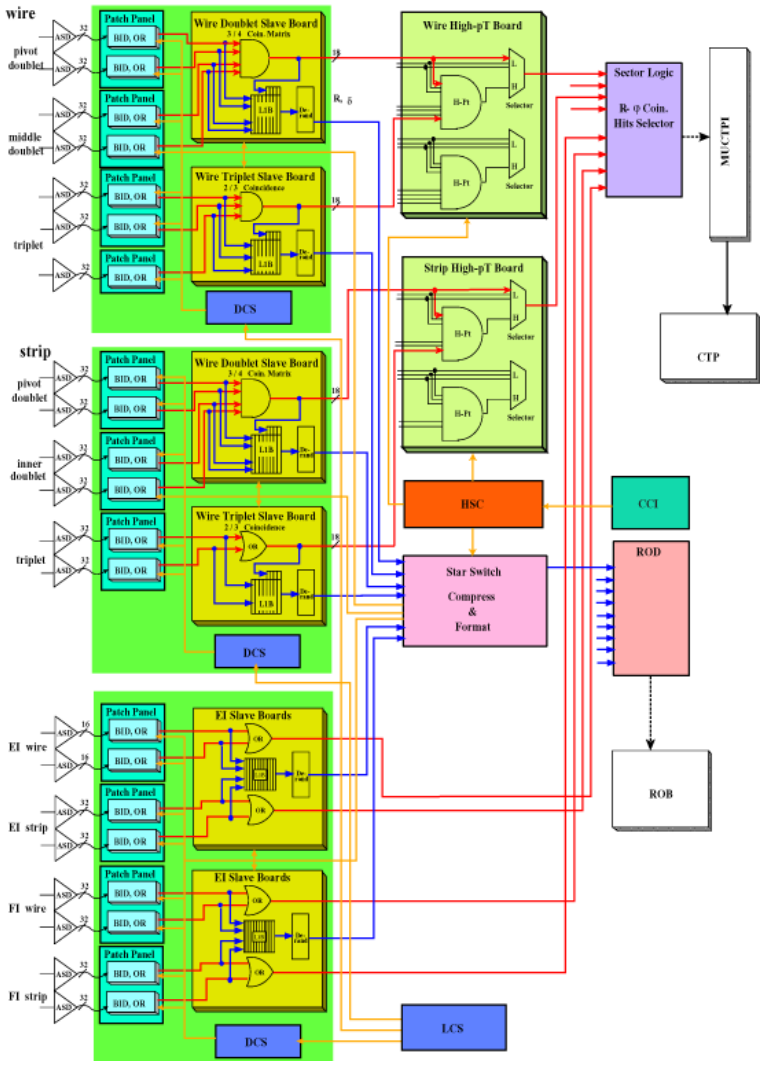

Figure 6.8: Overview of the TGC LVL1 Endcap Muon Trigger Electronics System

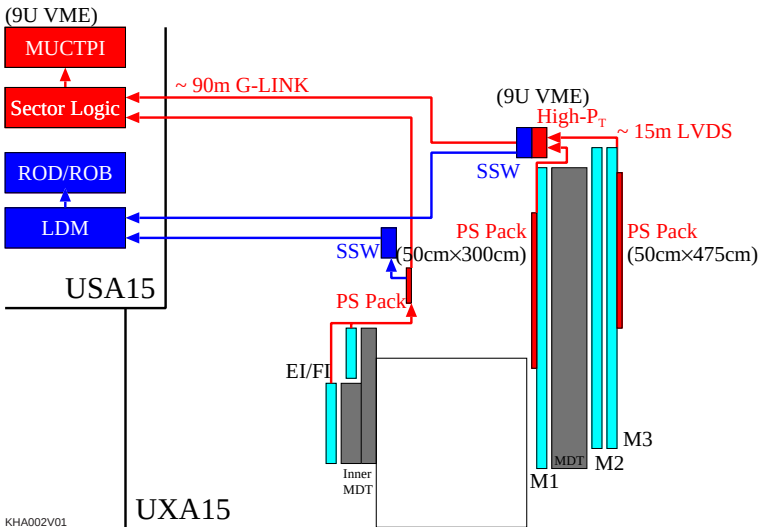

Figure 6.9: TGC electronics Placement

Output signals are sent to PS boards through twisted cables by using Low-voltage differential signaling (LVDS). The power, threshold voltage and test pulses for ASD boards are supplied from the PS boards.

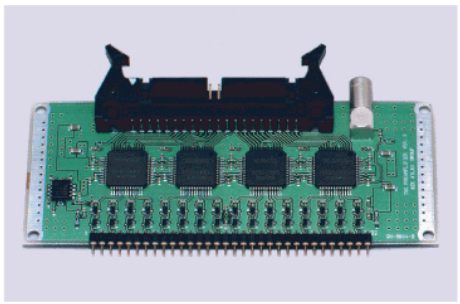

Figure 6.10: ASD Board

6.2.2 Patch Panel

The bunch crossing where a muon going through TGCs is produced should be identified by using timing information. In addition, signals need to be synchronized to take coincidences. However, signals from different positions arrive to PS boards in different timing because of differences on time of flight from the interaction point and cable propagation delay. The BCID for each hit signal is determined by the Patch Panel (PP) ASIC.

A block diagram of the PP ASIC is shown in Figure 6.11. At the first stage, LVDS receivers

followed by variable delays are implemented. One PP ASIC can handle 32 channels. The delay time can be varied in 32 steps and each step is 0.84 nsec. Hit signals can be masked out and/or asserted by using the MASK circuit. Then, signals are latched with the LHC clock to determine BCID. The output signals are synchronized with the clock. The signal will be sent after passing an OR logic to avoid the double count in the TGC overlap region.

Test pulses for ASD boards can be generated by the PP ASIC. The amplitude, width and timing of the test pulse can be varied. Parameters for delays, masks and test pulses are controlled by JTAG protocol.

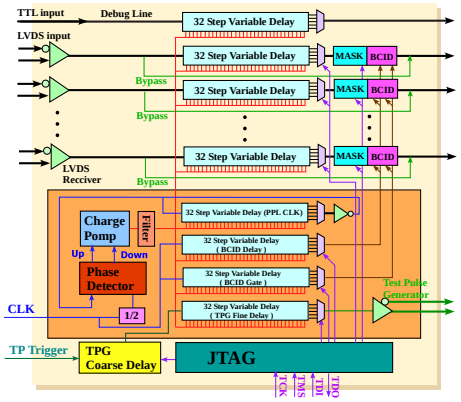

Figure 6.11: Block Diagram of PP ASIC

6.2.3 Slave Board (SLB) and 2 station coincidence

The SLB ASIC has two functional parts; trigger and readout.

In one SLB ASICs, 5 kinds of circuits are implemented; wire doublets, strip doublets, wire triplet, strip triplet and inner stations (EI/FI). Different coincidence circuits and corresponding encoding circuits are implemented.

Figure 6.12 show block diagrams of SLB ASICs for wire doublets. Each SLB covers 4 adjacent trigger sub-sectors. Signals from both M2 (middle) and M3 (pivot) doublets are fed into the 3 out 4 coincidences. The candidate with least sagitta is searched in two adjacent sub-sectors. Each output with position and sagitta information is encoded in 9 bits. The trigger part consists of phase adjusters, masks and coincidences. Phase adjust circuit is used to synchronize input signal timings. Mask circuits performs de-clustering consecutive hits, masking in/out and generating test pulses. Figure 6.16 shows de-clustering rule. If consecutive hit channels are detected, the second lowest number of

hit channels is selected.

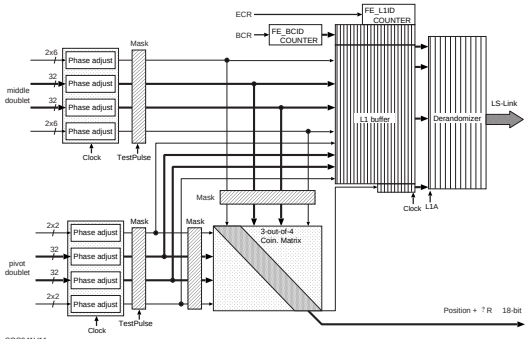

Figure 6.12: Block Diagram of 3 out of 4 SLB

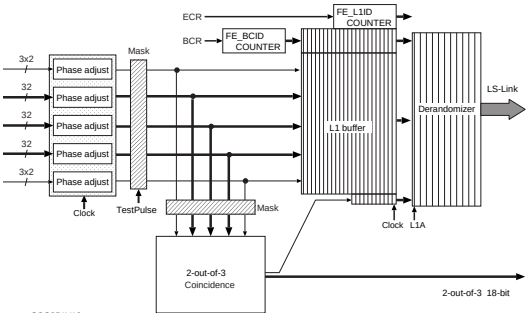

Figure 6.13: Block Diagram of 2 out of 3 SLB

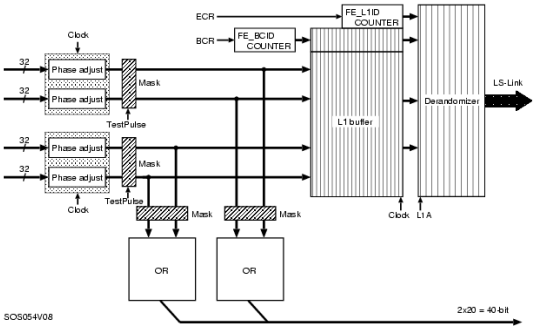

Figure 6.14: Block Diagram of 1 out of 2 SLB

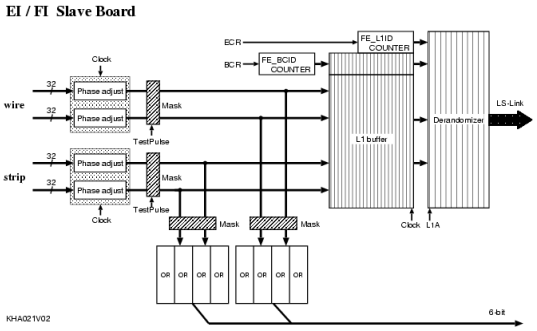

Figure 6.15: Block Diagram of EIFI SLB

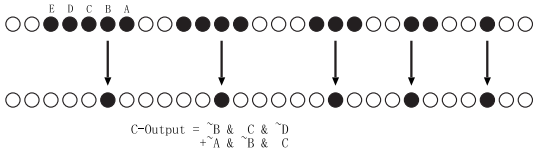

Figure 6.16: SLB Declustering Rule

The purpose of the readout part is to transfer inputs and outputs of the SLB for triggered events. The readout part consists of LVL1 buffer and derandomizer. The LVL1 buffer is a shift-register with 212 bits wide and 128 depth. 212 bits are further structed with 160 bits for input data, 40 bits for data of trigger line, and 12 bits of BCID. Data is kept until the L1A arrives. Data in 3 consecutive bunches (L1A timing, the previous BCID, and the next BCID) are transferred to the derandomizer, which sends data to the Star Switch together with 4bits of event counter via serial LVDS link.

6.2.4 High-Pt board (HPT) and 3 station coincidence

The HPT processes 3 station coincidence. The HPT board receives 2 station coincidence and triplet coincidence information to find muon track with 3 station coincidence. Three station coincidences can make better resolution than 2 station coincidences for measuring of sagitta. HPT ASIC calculates from the δR and $\delta\phi$ the curvature of muon track.

Wire and strip information are processed independently like 2station coincidence. Output information of HPT has three components; hit position on M3(pivot plane), sagitta value, and coincidence level. Coincidence level signify the track candidate if they filled requirements of 3 station coincidence or not. Each HPT ASICs find upto 2 candidates, 3 station coincidenced candidate is higher priority one.

An encoding circuit is implemented on HPT boards for strip. Strip HPT boards are implemented a HPT chip same as HPT for wire. This encoding circuit adjust the output information to fit the strip form.

G-Link is a kind of optical fiber. Output of HPT is adopted for the G-Link. HPT ASIC output the parallel data and it is converted a serial data which processed with G-Link serializer. Output data is sent to Sector Logic of the final step of TGC trigger electronics.

6.2.5 Sector Logic , R-ϕ coincidence

Sector Logic(SL) processes the final decision of the LVL1 Endcap Muon Trigger. SL has two important tasks; R-ϕ coincidences and track selection.

SL receives G-Link serialized optical signal from HPT modules. This signal is converted to parallel data on SL board.

Sector Logic handles both wire and strip data to finds and selects high p_T muon tracks using R-ϕ

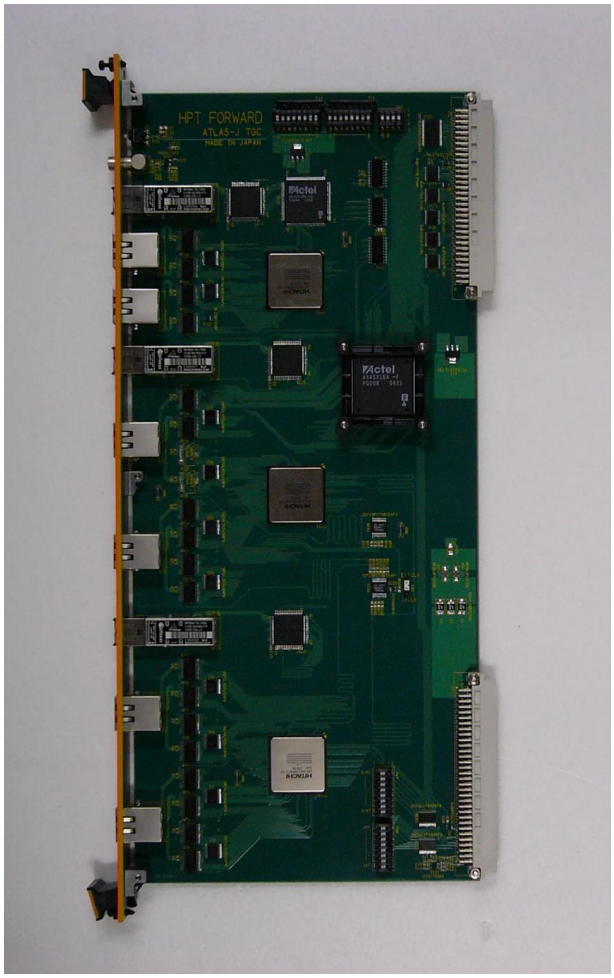

Figure 6.17: HPT Board

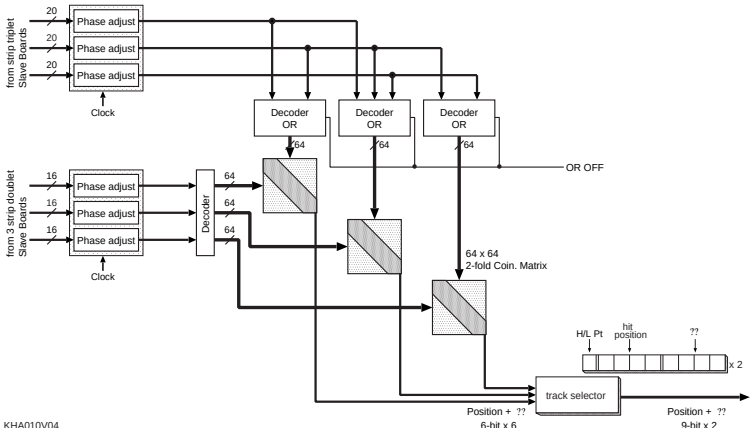

Figure 6.18: Block Diagram of HPT Wire

coincidence. Each trigger sector can provide up to two trigger candidates.

SL should select the highest p_T muon tracks. Track candidates are listed and they are sorted. p_T value to select the trigger candidate is discriminated number. Six level of p_T threshold is instituted on the scheme of LVL1 Muon Trigger. A combination menu of p_T threshold is defined by ATLAS experimental plan, which is changed by progress status of the experiment and condition of detector system. Sector Logic must be composed as a rewritable system to follow such chanse and apply a new logic.

An SL selects trigger candidates which have highest p_T threshold number. This determination of p_T threshold is processed with Coincidence Window. The Coincidence Window is a kind of look up table which consists of p_T threshold versus δR and $\delta\phi$. Sector Logic is designed to apply different pattern of Coincidence Window in each ROI.

If an SL finds more than three candidates, and their p_T threshold values are same number, then track candidates which found on small η ROI will be primary candidate. And if an SL find some trigger candidates on same η ROI, then the lowest ϕ ROI will be selected.

There are two output stream on SL. 34 pairs LVDS cable is adopted on SL board for trigger line output. This cable is connected to Muon Central Trigger Processor (MuCTPI).

CAT6 LVDS serial data will be sent to readout line. An SLB is adopted on a trigger sector.

More detail of functionality will be presented on next chapter.

CLOCK	Provided from LHC or ATLAS detector system or LTP on each subsystems.
L1A	Level1 Accept. This signal is issued from CTP or LTP on each subsytems.
BCR	BCID Reset signal.
ECR	Event Counter Reset.
EVID(L1ID)	EVent IDentifier.
BCID	Bunch Crossing ID.

Table 6.1: TTC signals

6.2.6 SSW

Star Switch(SSW) module supports the readout process. This module send the data, which are retrieved from SLB ASICs, to Readout driver module (ROD). An SSW manages up to 23 SLBs. SSW formats the readout data and serialize to optical signal. And SSWs configures PP ASICs and SLB ASICs. Cat6 LVDS cable is connected for the communication between SLB and SSW.

6.2.7 TTC

Timing, Trigger and Control distribution (TTC) [24] is a system which used in all ATLAS system. Purpose of this system is to provide some signals to establish a coherence of process between all Front End electronics. TTC can provide clock and L1A to each sub systems. In addition TTC can be handled and executed a test and a calibration command.

Chapter 7

The Sector Logic

Sector Logic is the final part of LVL1 Endcap Muon Trigger decision as already described. SLs are installed at a counting room USA15 in ATLAS cavern area to avoid hard radiation. USA15 is 100m away from experimental hole of UX15.

This chapter describs about hardware implementation and functions of Sector Logic.

7.1 Requirments

Required functions of SectorLogic are listed as following.

- Measure the transverse momentum and position of a track using wire and strip information. And select up to two muon candidates with highest p_T in each trigger sector.
- Classify the muon candidate into six levels according to measured p_T.
- Determine the ROI of the muon candidate based on measured position.
- Provide the BCID which the muon candidate belongs to.
- Process without deadtime as other LVL1 Endcap Muon Trigger electronics.

To fulfill these requirements, Sector Logic is designed using pipeline structure for the deadtime less processing; the Coincidence Window is applied for measurements of track p_T, rewritable Field Programmable Gate Aray(FPGA)s are adopted to update the Coincidence Window and trigger algorithm, and synchronized with other parts of LVL1 Endcap Muon Trigger System via TTC.

7.2 Board Design

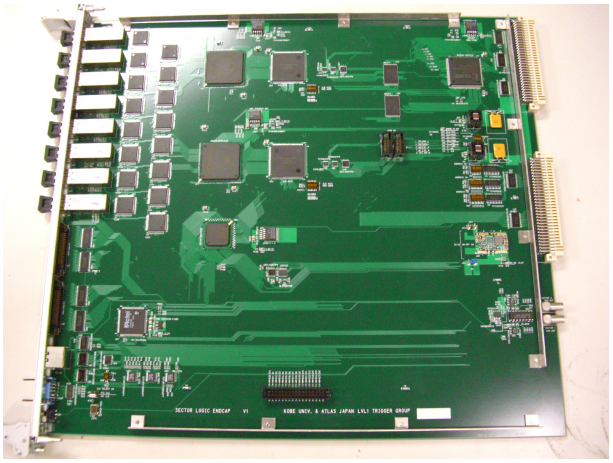

Figure 7.1: Sector Logic Board

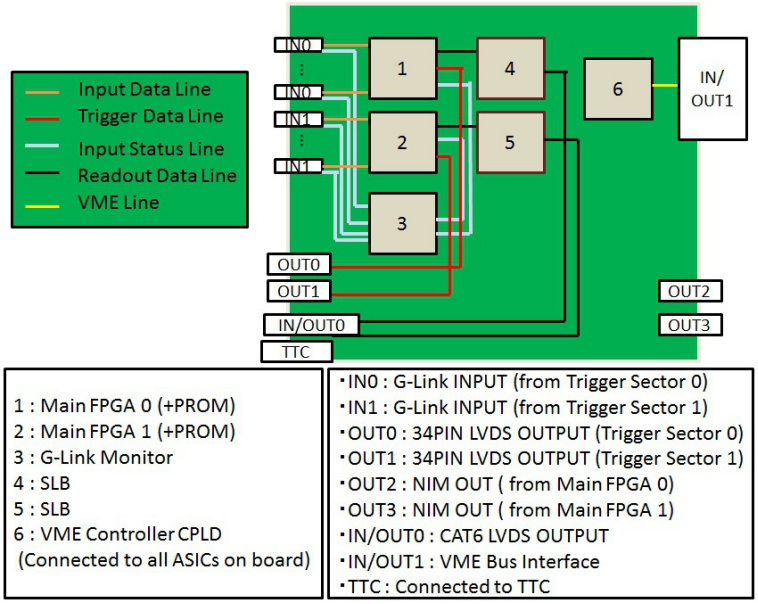

Figure 7.2: Diagram of SL Board

In this subsection, functions implemented on SL board will are overviewed.

The Sector Logic board is a 9U VME module (Figure 7.1). An SL board handles 2 trigger sectors. Several components are listed below mounted on SL to fulfill the requirements

- Main FPGA (2 /board)
- G-Link Input (Endcap: 16 /board, Forward: 6 /board)

- G-Link Monitor (1 /board)
- 34-pairs LVDS Output (2 /board)
- SLB ASIC (2 /board)
- LDVS In/Out (CAT6) (1 /board)
- VME Controller CPLD (1 /board)
- TTC input (1 /board)
- NIM Out (2 /board)

Main FPGA processes the logic of trigger decision using input signals provided from HPT. Optical receivers and following G-Link de-serializers are mounted to receive trigger information from HPT modules. An FPGA, called "G-Link Monitor", is mounted to watch and control the status of G-Link de-serializers. The information of selected muon candidates are sent to MuCTPI through 34-pairs LVDS outputs. Information of HPT and muon candidates are sent to a SLB ASIC [27] for readout. After receiving L1A for triggered events, the SLB sends information to a SSW via CAT6 LVDS input/output. FPGAs mounted on the Sector Logic can be configured via VME protocol on the backplane. A CPLD (Complex Programmable Logic Device) [31] called as "VME Controller CPLD" takes care of VME protocols. The Sector Logic board should be synchronized with other parts of Endcap Muon Trigger system via TTC. TTC signals from a TTC-rx chip are distributed to sector logic board by using LVDS. The Sector Logic can provide a NIM output, which is used a source of L1A for standalone operation of the LVl1 Endcap Muon system.

7.2.1 Main FPGA

Virtex-II families by Xilinx are adopted for the main FPGAs on the SL because these were the highest performance FPGA when we started design of the Sector Logic.

The chip type is selected based on capacity of RAM memories enough for the LUT (Coincidence Window). Xilinx VirtexII VC2V3000 [29] is used for Endcap, and VirtexII VC2V1000 [29] is used for Forward. The detail of LUT is described later in section 7.4.2. This FPGA can be re-configured from VME. Configuration of FPGA is lost when power is cut, and Main FPGA must be configured by VME. Detailed functions and implementations are described later in section 7.3

7.2.2 G-Link input

G-Link [36] protocol through optical fibers is adopted for a connection between HPT and Sector Logic. Agilent HDMP1032 chip is adopted as a transmitter on the HPT and it serializes trigger data. An optical transmitter of V23818 [33] is mounted on the HPT and optical receiver M2R-25-4-1-TL Optical Gigabit Ethernet(Endcap [34]) or V23818-K305-L57 (Forward [35]) is used for optical receiver on the SL. An serial to parallel converter of HDMP1034 is adopted as a G-Link receiver. These HDMP chips are operated with 40.08 MHz LHC clock, though chips can work with wide clock range of 13-70 MHz. The range bit of HDMP chips nead to be set properly according to operation frequency. The clock range can be selected in three different mode, as listed below;

Range 1 : 13MHz to 26MHz

Range 2 : 20MHz to 45MHz

Range 3 : 40MHz to 70MHz

G-Link communicats 20bit word between transmitter and receiver. The word consists of 16bit word field and 4bit code field. G-Link can send 16bit word and 1bit "flag" information, 1 bit flag is determined by the pattern of code field. Flag information is used as 17th bit datum (16bit word + 1bit flag information). G-Link can be operated in three types of communication mode; Data mode, Control mode, and Idle mode. Data mode handles full bit of data mode, Controle mode handles 14bit word field(in the case of SL, this function is not used.), and Idle mode is operated to establish the link between transmitter and receiver.

HDMP1034 has four status signals; RXDATA, RXCTRL, RXERROR, and RXREADY.

- RXDATA : Indicates G-Link communication mode is set in Data mode
- RXCTRL : Indicates G-Link communication mode is set in Control mode
- RXERROR : Indicates G-Link communication fails
- RXREADY : Indicates G-Link communication works correctly for recent 64(-128) CLKs.

Three G-Link inputs are used to receive HPT signals in a Forward sector (6 G-Link chips are mounted on a Forward board). Six G-Link inputs are used for HPT signals in an Endcap sector, and additional 4 G-Link inputs for EI/FI signals are mounted. In total, there are 16 G-Link inputs on an Endcap board.

7.2.3 Glink Monitor FPGA

Xilinx Spartan2E XC2S150E [30] for Endcap and Xilinx Spartan2E XC2S50E for Forward are adopted to monitor the G-Link state. This Glink Monitor FPGA sets the clock range, and receives four status signals of RXDATA, RXCNTL, RXERROR, RXREADY from each HDMP1034. It also asserts G-Link Fine, a status flag sent to the main FPGA, if all following conditions are fulfilled.

- The connection state is properly locked in DATA mode(RXDATA is high,RXCNTL is low, RXERROR is low, RXREADY is high for all HDMP1034 chips on the sector)
- Main FPGA is not requesting the input chip reset.
- Glink Monitor are not in recovering procedure.

7.2.3.1 Recovering Procedure

The G-Link Fine flag indicates any errors on a G-Link chip. To identify the problematic input among 16 inputs for Endcap (6 for Forward), the Main FPGA checks data pattern from HPT continuously. Main FPGA asks G-link Monitor to recover problematic G-Link inputs. When Glink Monitor receives the recovering request, Glink Monitor waits automatic recovery during 16 clocks. If the chip can not recovered from the error, G-Link monitor goes into re-set procedures by changing the clock range setting of HDMP1034 from range 2 (20-45MHz) to range 1 (13-26 MHz). HDMP1034 will not able to establish link because configured clock range is not matched with given clock frequency provided by TTC. The G-Link Monitor waits until the G-Link chip goes into error state after about 30,000 clocks. G-link Monitor keeps the error state for 1 million clocks and then set the proper clock range.

7.2.4 LVDS Output

All SL boards are connected to MuCTPI. An SL board has two 34-pairs LVDS cable connectors, and each of them corresponds to one sector.Assignment of the LVDS cable is shown in table 7.1, while other 2 PINs are connected to GND. The trigger information consists of ROI, p_T threshold, sign which means the track bending of δR being positive or negative, and "morethan2" flag which means the triggered event contains more than 2 candidates or not (This flag function is disabled now).

ROI and p_T threshold and sign information are sent two candidates.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Endcap	S2	S1	BC			NA		$p_T(2^{nd})$			$p_T(1^{(st)})$			NA	ROI(2^{nd})									NA	ROI(1^{st})								M
Forward	S2	S1	BC			NA		$p_T(2^{nd})$			$p_T(1^{(st)})$			NA				ROI(2^{nd})					NA				ROI(1^{st})					M

Table 7.1: Assignment of SL Trigger Information in 34-pairs LVDS cable (send to MuCTPI). ”S” is the sign bit, BC is the BCID which width is 3bits, and M is a flag of the morethan 2 candidates.

7.2.5 SLB and Cat6 LVDS in/out

Two SLBs are mounted on an SL board to readout the input/output data. An SLB covers a trigger sector. The readout data consists of trigger information sent to MuCTPI, G-Link Fine flag (as mentioned in section 7.2.3), input data from HPT chips, and the EI/FI hit information only for Endcap. An SLB can provide upto 160 bit of readout data to SSW. These information are arranged by Main FPGA. Figure 7.3 and 7.4 are bitmap matrix of readout data (output). The bit address is assigned as follows; vertical cells are pointed i and horizontal cells are pointed j, then a cell address C_{ij} is assigned $(8 \times i + j)$th bit. The detail of readout data are; blue colored cells are trigger information, Glink Fine shows G-Link state if it shows no problem then this flag become 0, green colored information are HPT wire of 1st candidate, yellow colored information are 2nd candidate, pink colored information are HPT strip of 1st candidate, gray colored are 2nd candidate, dark blue cells are hit information of EI/FI. If an SL has no trigger information, then all readout data become 0.

7.2.6 VME Controller CPLD

The Sector Logic is implemented as a VME 9U board and the VME controller CPLD handles control lines on the VME backplane. A CPLD of ”Xilinx COOL RUNNER” is mounted on board for VME operation. This chip can work immediately on system boot up because CPLD utilizes non volatile configuration memory. As described before, configuration and settings for FPGAs on the SL (Two Main FPGAs, G-Link Monitor) can be performed via VME protocol. So, all FPGA as well as this VME controller CPLD are mapped in VME address. Table 7.2 shows the address mapping, where chip address is shown on Table 7.3.

CELL add	0	1	2	3	4	5	6	7
0	Morethan2	ROI1<0>	ROI1<1>	ROI1<2>	ROI1<3>	ROI1<4>	ROI1<5>	ROI1<6>
1	ROI1<7>	1	ROI2<0>	ROI2<1>	ROI2<2>	ROI2<3>	ROI2<4>	ROI2<5>
2	ROI2<6>	ROI2<7>	1	PT1<0>	PT1<1>	PT1<2>	PT2<0>	PT2<1>
3	PT2<2>	1	1	BCID<0>	BCID<1>	BCID<2>	Charge1	Charge2
4	Glink Fine	0	0	0	0	0	0	0
5	Wire0 dR1<0>	Wire0 dR1<1>	Wire0 dR1<2>	Wire0 dR1<3>	Wire0 Sign1	Wire0 H/L1	Wire0 Pos1	0
6	Wire1 dR2<0>	Wire1 dR2<1>	Wire1 dR2<2>	Wire1 dR2<3>	Wire1 Sign2	Wire1 H/L2	Wire1 Pos2	Wire1 ID2<0>
7	Wire1 ID2<1>	Wire1 ID2<2>	Wire1 dR1<0>	Wire1 dR1<1>	Wire1 dR1<2>	Wire1 dR1<3>	Wire1 Sign1	Wire1 H/L1
8	Wire1 Pos1	Wire1 ID1<0>	Wire1 ID1<1>	Wire1 ID1<2>	Wire2 dR2<0>	Wire2 dR2<1>	Wire2 dR2<2>	Wire2 dR2<3>
9	Wire2 Sign2	Wire2 H/L2	Wire2 Pos2	Wire2 ID2<0>	Wire2 ID2<1>	Wire2 ID2<2>	Wire2 dR1<0>	Wire2 dR1<1>
10	Wire2 dR1<2>	Wire3 dR1<3>	Wire2 Sign1	Wire2 H/L1	Wire2 Pos1	Wire2 ID1<0>	Wire2 ID1<1>	Wire2 ID1<2>
11	Wire3 dR2<0>	Wire3 dR2<1>	Wire3 dR2<2>	Wire3 dR2<3>	Wire3 Sign2	Wire3 H/L2	Wire3 Pos2	Wire3 ID2<0>
12	Wire3 ID2<1>	Wire3 ID2<2>	Wire3 dR1<0>	Wire3 dR1<1>	Wire3 dR1<2>	Wire3 dR1<3>	Wire3 Sign1	Wire3 H/L1
13	Wire3 Pos1	Wire3 ID1<0>	Wire3 ID1<1>	Wire3 ID1<2>	0	0	0	0
14	Strip0 dPhi2<0>	Strip0 dPhi2<1>	Strip0 dPhi2<2>	Strip0 sign2	Strip0 H/L2	Strip0 Pos2	Strip0 ID2<0>	Strip0 ID2<1>
15	Strip0 ID2<2>	Strip0 dPhi1<0>	Strip0 dPhi1<1>	Strip0 dPhi1<2>	Strip0 sign1	Strip0 H/L1	Strip0 Pos1	Strip0 ID1<0>
16	Strip0 ID1<1>	Strip0 ID1<2>	0	0	0	0	0	0
17	Strip1 dPhi2<0>	Strip1 dPhi2<1>	Strip1 dPhi2<2>	Strip1 sign2	Strip1 H/L2	Strip1 Pos2	Strip1 ID2<0>	Strip1 ID2<1>
18	Strip1 dPhi1<0>	Strip1 dPhi1<1>	Strip1 dPhi1<2>	Strip1 sign1	Strip1 H/L1	Strip1 Pos1	Strip1 ID1<0>	Strip1 ID1<1>
19	EI/FI<0>	EI/FI<1>	EI/FI<2>	EI/FI<3>	EI/FI<4>	EI/FI<5>	EI/FI<6>	EI/FI<7>

Figure 7.3: SL Readout Matrix for Endcap.

CELL add	0	1	2	3	4	5	6	7
0	Morethan2	ROI1<0>	ROI1<1>	ROI1<2>	ROI1<3>	ROI1<4>	ROI1<5>	1
1	1	1	ROI2<0>	ROI2<1>	ROI2<2>	ROI2<3>	ROI2<4>	ROI2<5>
2	1	1	1	PT1<0>	PT1<1>	PT1<2>	PT2<0>	PT2<1>
3	PT<2>	1	1	BCID<0>	BCID<1>	BCID<2>	Charge1	Charge2
4	Glink Fine	0	0	0	0	0	0	0
5	Chip0 dR2<0>	Chip0 dR2<1>	Chip0 dR2<2>	Chip0 dR2<3>	Chip0 Sign2	Chip0 H/L2	Chip0 Pos2	Chip0 ID2<0>
6	Chip0 ID2<1>	Chip0 ID2<2>	Chip0 dR1<0>	Chip0 dR1<1>	Chip0 dR1<2>	Chip0 dR1<3>	Chip0 Sign1	Chip0 H/L1
7	Chip0 Pos1	Chip0 ID1<0>	Chip0 ID1<1>	Chip0 ID1<2>	0	0	0	0
8	Chip1 dR2<0>	Chip1 dR2<1>	Chip1 dR2<2>	Chip1 dR2<2>	Chip1 Sign2	Chip1 H/L2	Chip1 Pos2	Chip1 ID2<0>
9	Chip1 dR1<0>	Chip1 dR1<1>	Chip1 dR1<2>	Chip1 dR1<2>	Chip1 Sign1	Chip1 H/L1	Chip1 Pos1	Chip1 ID1<0>
10	Chip2 dPhi2<0>	Chip2 dPhi2<1>	Chip2 dPhi2<2>	Chip2 Sign2	Chip2 H/L2	Chip2 Pos2	Chip2 ID2<0>	0
11	Chip2 dPhi1<0>	Chip2 dPhi1<1>	Chip2 dPhi1<2>	Chip2 Sign1	Chip2 H/L1	Chip2 Pos1	Chip2 ID1<0>	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0

Figure 7.4: SL Readout Matrix for Forward.

7.2.7 TTC input

A TTCrx is installed in a VME crate as an SL board. This TTCrx sends these signals for SL boards installed in same VME crate.

- Clock (to CPLD,All FPGA,SLB,G-Link)
- BCR [1] (to All FPGA,SLB)
- L1A [2] (to All FPGA,SLB)

[1] Bunch Counter Reset

[2] Level1 Accept

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	A	A	A	A	0	0	B	B	0	0	0	C	0	0	0	0	D	D	0	E	E	E	E	E	E	E	E	E

Table 7.2: VME Address Space for SL. Address space A indicates the number of 1/12 sector (0x1 to 0xc), B indicates Endcap or Forward (Endcap:2'b11, Forward:2'b10), C indicates the ϕ number for SL board (Endcap ϕ0/1:1'b0, ϕ2/3:1'b1, Forward:1'b0), D indicates the ASIC address(table7.3), and E indicates register address.

ASIC	Address
VME Controller CPLD	0x0
Main FPGA0	0x1
Main FPGA1	0x2
G-Link Monitor FPGA	0x3

Table 7.3: VME Address for chips on SL

- ECR [3](to All FPGA,SLB)
- RESET (to Main FPGA,SLB,CPLD)

7.2.8 NIM output

One Main FPGA is connected to one NIM output terminal. This NIM output can use as LVL1 trigger for local test environment.

7.3 Algorithm of Main Trigger Process

This section will present the detailed algorithm of Main FPGA's functions and how they are implement. The block diagram of the Sector Logic is shown in Figure 7.5.

The first stage is input delay, where input signals are delayed in a unit of a half clock to align all HPT information. At the second step, Decorder block translates HPT data to get position, δR/$\delta\phi$ and H/L information. Then, the Decorder block distributes the δR/$\delta\phi$ and H/L information to the corresponding SSC block. In each SSC block according to the position information, one muon candidate with p_T level is searched by using the Coincidence Window. Then, the Track Selector picks up two

[3]Event Counter Reset

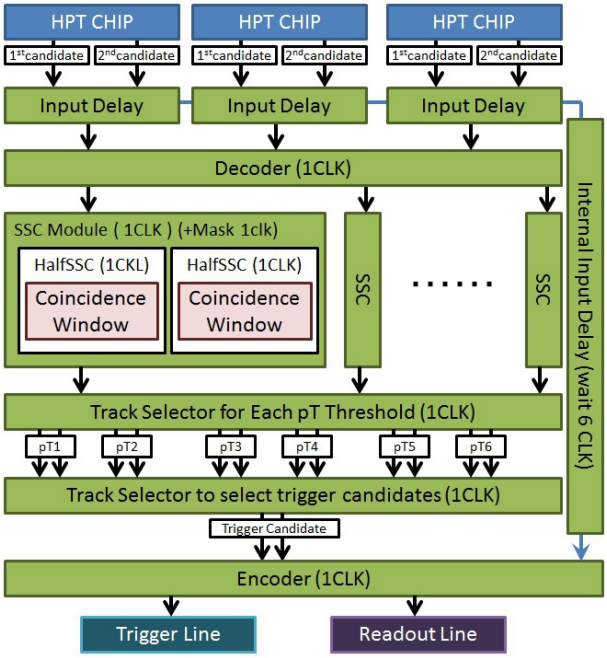

Figure 7.5: SL Trigger Step

muon candidates with highest p_T among all candidates from all SSC blocks. Encoder arrange output information for MuCTPI and SLB on SL. Output for MuCTPI is trigger line, SLB on SL is readout line.

7.3.1 HPT Input Information

An Endcap Sector Logic receives trigger information from four HPT wire chips and two HPT strip chips. A Forward SL receives trigger information from two HPT wire chips and one HPT strip chip.(Figure 7.6) Each HPT chip sends two candidates at maximum. The HPT information consists of Hit ID, pos flag, H/L flag, sign, and delta values. (Table 7.7) Hit ID and pos flag are position information. Hit ID coresponds 2 ROIs for each element, and pos flag indicates the exact ROI in confined region. H/L information is the coincidence level. Sign and delta value means the curvature of track candidate. δR has the width of 4bits, and $\delta\phi$ has the width of 3 bits. (The sign is mentioned as 7.2.4) These information is used to determine the track p_T level with Coincidence Window.

7.3.2 Input Delay

G-Link chips on both HPTs and SLs works with LHC clock. But, clock phase may differ for board by board. In addition, length of optical cables, about 100m between UX15 and USA15, may differ. If the clock latch timing is set in bad phase, then SL will not receive input signals in correct form. Thus timing need to be adjusted to synchronize input data. The latch timing for the input data can be changed in an unit of half clock, and latched data can be delayed up to 2 clocks. The latched timing and delay value can be set by using VME access. To confirm the latch phase and delay timing, test signals are used. All SLBs issue test signals with a track pattern in the same BCID (i.e once per orbit) and send them to HPT boards. HPT boards send a candidate to the SL. Then, input data on the SL is tested to check whether settings for Input Delay block are correct.

7.3.3 Decoder

Each HPT data is decoded to get position information from Hit ID fields.(as mentioned in section 7.3.1) However, not all bits from HPT are sent to the Sector Logic. Some bits of Hit ID are omitted to reduce number of optical links.

No data will be sent to the next stage in case of G-Link error (i.e. G-Link Fine flag set to low).

7.3.3.1 Endcap HPT strip bug

Endcap Sector Logic is connected to two HPT chips for strip. One of them placed η number 4 and 5 on pivot plane (this numbering is mentioned in section 6.1.1), HitID is assigned to 0 and 1 for lower η , 4 and 5 for higher η. However, the MSB of HitID is not sent to the SL by mistake (Wrong wiring on HPT borads for strip). We can not distinguish these two chambers. So, trigger information is sent to SSC blocks for both chambers. This problem may cause fake trigger. Suppose that one muon flys into each chamber of number 4 and 5. Because of the bug, each chamber has one wire candidate and

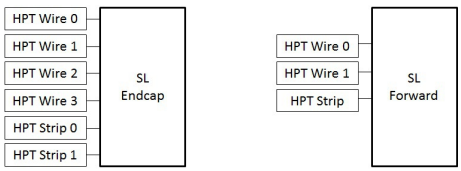

Figure 7.6: HPT SL Connection

bit	9	8	7	6	5	4	3	2	1	0
wire	Hit ID			POS	H/L	Sign	δR			
strip	NA	Hit ID		POS	H/L	Sign	$\delta\phi$			

Figure 7.7: Input information

two strip candidates. If wrong pair is selected, the trigger can be issued with wrong p_T higher than the real one. Such a multiple muon rarely occur at the current luminosity and does not result in serious problems.

7.3.4 Sub Sector Cluster (SSC)

Sub Sector Cluster is a kind of jargon for TGC SL. SSC covers two ROI for η direction, and four ROI for ϕ direction. There are 19 SSCs for Endcap and 8 SSCs for Forward. SSCs are numbered starting with small eta.(i.e SSC0 is the outermost)

A half-SSC covers 2(η)×2(ϕ) ROIs. Only one candidate is selected by each SLB coincidence. So, half-SSC takes care of one pair of wire and strip HPT candidates. It means that each half-SSC determine only one candidate with p_T by using the Coincidence Window. Two half-SSCs in a SSC shares the same wire candidate. So, the candidate with higher p_T is selected among two half-SSCs. (candidate with smaller ϕ is selected if both has the same p_T)

7.3.4.1 Half-SSC

Half-SSC block is a part of SSC block. Each Half-SSC process the R-ϕ coincidence to find a trigger candidate and determine the p_T threshold. LUT, represents the Coincidence Window is applied on this module. p_T threshold information has the width of 3 bits, and the 1 bit information of sign (introduced in section 7.2.4) are given.

7.3.4.2 Handling about Chamber Boundary

One candidate from wire HPT and two candidates from strip HPT are fed into a SSC. However, some SSCs in Endcap cover chamber overlap region.(SSC2,4,6,and 12) In these SSCs, strip HPT candidates from both chambers should be taken into account.

- The candidate with 3-station coincidence (i.e. H/L bit is high) is superior to one with 2-station coincidence
- The candidate for the chamber which has more wires for the SSC is superior. For example, the candidate for chamber of number 2 overcomes one for the chamber number 1 in SSC2. There are some possibility to trigger non boundary ROI in boundary SSC using strip information issued from another chamber.

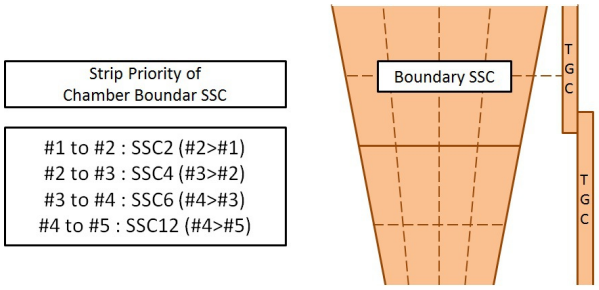

Figure 7.8: Strip Priority about Chamber Boundary SSC

7.3.5 Track Selector

Track Selector picks up up to two trigger candidates among 19 (8) candidates from SSCs for Endcap (Forward).

The schematics of track selector is shown in Figure 7.9. Track Selector consists of two parts; in the first part, named Pre-Selector up to two candidates are selected in each p_T threshold, and the second part named Final-Selector, selects upto two highest priority candidates from among the result of first part.

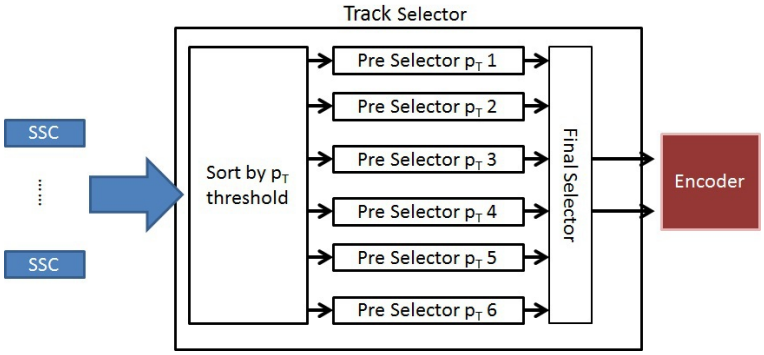

Figure 7.9: Track Selector

7.3.5.1 Pre-Selector

In this stage, trigger candidates are sorted by p_T levels and sent to the Pre-Selector with corresponding p_T level. Each Pre-Selector picks up upto two candidates from the SSC for lowest η's. The selecting process can be divided for two part. Each part are processed by same type of priority encoder. At first, priority encoder selects the highest priority SSC. Detailed position information to

determine the ROI is kept in a register. After selecting the SSC of first candidate, the second candidate will be selected with the result of first candidate. At the process to select the second candidate, the priority encoder receives data which refer to the result of first candidate selection.

7.3.5.2 Final-Selector

Final-Selector picks up up to two candidates. This selection is processed by a priority encoder which is different of Pre-Selector's one. This priority encoder receives input information and returns fixed result of selection. All patterns of input vs output is pre-described. This process is executed by only one step and this implementation occupies many memory but consumes shorter time than Pre-Selector's one.

7.3.6 Encoder

This module makes output of Trigger Line (to MuCTPI) and Readout Line (to SLB on SL board).

Inputs are p_T threshold and ROI information from Track Selector, and Bunch Counter Reset(BCR) signal from TTC.

7.3.6.1 BCID

Three bit BCID counter is equipped with the Sector Logic and it is synchronized to the LHC bunch number by using BCR signal. The counter is reset after BCR signal is delayed. LHC has 3564bunch. then the maximum BCR delay is to be 3564 clock.

7.3.7 Internal Input Delay

The input data should be synchronized with the trigger information from Final Selector. This block, which is implemented as FIFO, keeps input data for six clocks.

7.4 Implementation

In this section, the implemention of the trigger logic to FPGAs and CPLD on SL board will be presented. The logic of FPGAs and CPLD are described in verilog HDL. One of FPGA functions of LUT is introduced, and how to implement the Coincidence Window to FPGA will be described. The preparation procedure of the logic of Main FPGA will be presented in this section.

7.4.1 Verilog HDL

Verilog is one of Hardware Description Language (HDL). Components of verilog code can be classified into two kinds of files. Verilog file (.v) is a logic code file. PIN assign, and pattern of LUT (section 7.4.2) are described in user constraint file (.ucf). The construction of verilog code is shown in Figure 7.10. The Verilog compiler and related tools are distributed by device manufactures. For our application, Xilinx ISE is used. This software has three compilation (1) Logic synthesis: a schematic diagram of gate circuits is generated only from Verilog files (i.e. constraint files are not used) (2) Place & Route: detailed layout of circuits (wireing and timing optimization) on FPGA is determined by taking into account constraint files (3) Bitmap generation:a bitmap file for configuration of FPGA is generated.

A logic synthesis software ”Synplify” provided by Synopsis Corporation is used at the first step, especially for the case of Main FPGA because standalone ISE can not handle a function of LUT. Synplify enables ISE to handle LUT. From here, the discussion is fucused on the Main FPGA. The compilation task of verilog HDL can be executed by using GUI on ISE or command line. GUI enables us to use complex configuration, while command line enables us to process automatically. It is, however, difficult to use Synplify via command lines, because it is not contained in ISE. The first step, logic synthesize can be executed from only GUI. The second step and third step are executed using command line. Each bitmap file is generated from several Verilog files and one constraint file. One bitmap file is used to configure one FPGA chip. The maximum number of bitmap files is 144 (total number of trigger sectors).

7.4.2 LUT

Look Up Table is one of functions of VertexⅡ-FPGA. It takes only one clock to access the LUT. An LUT has 12bits input and 4bits outputs. Initial data in the LUT can be set by using constraint file (i.e. ucf). Memory size required for the SL and capacity of LUT are listed on Table 7.4.

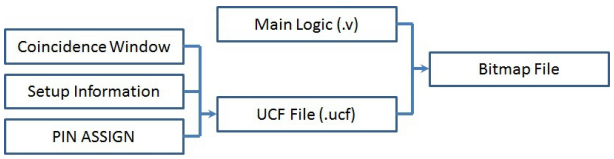

Figure 7.10: Relation of Files and Information for Verilog HDL

	Type of FPGA	Capacity of Memory	Required Memory
Forward	XC1000-BG575	720kb	576kb
Endcap	XC3000-BG728	1728kb	1656kb

Table 7.4: Required Memory and Capacity of LUT

7.4.3 Implementation of the Coincidence Window

This subsection introduces how to implement the Coincidence Window. Coincidence Window is implemented in Main FPGA as a function of LUT. Coincidence Window is described in a text database file(.db). A Coincidence Window is prepared for each ROI, and a database file contains a set of Coincidence Windows in a trigger sector. A ucf file is generated from a database file. How to prepare ucf file, and how to prepare enough number of set of bitmap files is described below.

7.4.3.1 Database File

Allocation of set of coincidence window is identified by side information, octant ID, and module ID. They are the identification information of database file.

An octant covers eight divided region in each Big Wheel (section 5.2.2). An octant consists of a set of nine modules. A module ID is assigned as a trigger sector in an octant like Figure 7.11. Module ID 0,1,3,4,6,7 are allocated on Endcap region, and module ID 2,5,8 are allocated on Forward region.

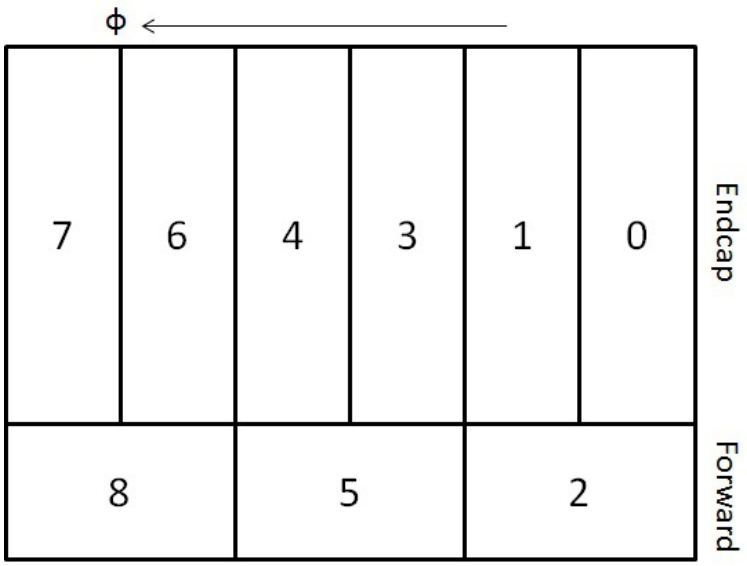

Figure 7.11: Allocation of Module ID

7.4.4 DBtoUCFconverter

This is one of the SL preparation tools, which have been developed by us. The role of this tool is to convert a database file to an ucf file. DBtoUCFconverter is a program written by C++. This tool reads text file which contains some information included in ucf file;

- Coincidence Window (Database file name)
- PIN assign setup for FPGA (Described in ucf file)
- Date, logic version, setup, trigger menu information (Described in ucf file)

7.4.5 BitfileMaker

Xilinx ISE utilizes several executable files (.exe)[32] to generate a bitmap file from a schematic design. These files can be executed from command line. BitfileMaker executes the second step and the third step of compilation (section 7.4.1). The second step are; NGD build, Map, Par. And third step is executed by Bitgen. The detail is listed as following;

- NGD build : make a ”Net Generic Database (NGD) file” from ISE project file and ucf file.

- Map : do the mapping of Logic cell, I.O cell, other components on logic after checking ”design rules” for a NGD file. As a result, a NCD file will be generated.

- Par : do ”Place & Route” step based on the NCD file created by Map. Par puts logic units and wiring between them on the device and create another NCD file including floor plan.

- Bitgen: Generate a bitmap file from the NCD file from Par.

BitfileMaker read a setup text, and starts the sequence. Pick up an ucf file in a storage of ucf file, and make a bitmap file using base of schematics and ucf file. This sequence continues until all bitmap files are generated.The bitmap generation takes about 2 hours for one octant.

7.5 Other Functionalities in Main Process FPGA

This section presents functions implemented in Main FPGA to support the configuration and monitor the process. LUT version reader is a function to support the configuration. Input checker, scaler, and mask are implemented for monitoring and modify the experiment state. These optional functions can be set and read through VME.

7.5.1 LUT Version Reader

Version information is used to identify the implemented logic in Main FPGA. This information is implemented as a LUT which can be read through VME. The version information consists of; side, octnat number, Module ID, FPGA number, mask, p_T threshold for each p_T level, and date information (detail is listed on Table 7.5). Mask information shows the setup about ”High-Low mask for R coincidence”, ”High-Low mask for ϕ coincidence”, ”R-ϕ dummy”, and p_T mask (Table 7.6). Prepared bit width is 32 but used number of bits is 16, because each mask information uses 4 bits. Detail of bit assign about H/L mask for R (ϕ) are; the lowest bit means reject 2station coincidence, and second lowest bit means reject 3station coincidence. Detail of bit assign about R-ϕ dummy are; the lowset bit means dummy ϕ coincidence is applied, and second lowest bit means dummy R coincidence. Masks will be applied at the making of Coincidence Window.

In configuration of the SL, version information is compared with the reference to confirm if the correct file is downloaded in individual FPGA.

Information	Bit Length	Detail
side	4	A side:"a", C side:"c", setup for common about side:"0"
octant number	4	"0" to "8, setup for common about octant:"0"
Module ID	4	Module ID:0 to 8
FPGA number	4	FPGA location on each board.
Mask	32	Setup about H/L Mask(R), H/L Mask(ϕ), R/ϕ dummy, p_T mask.
p_T Threshold	8/level	p_T value (in unit of GeV/c) for each threshold.
Date information	32	The date of when the ucf file is generated.

Table 7.5: Version Information

High-Low Mask (R)	Disable the trigger with R 3-station or 2-station coincidence
High-Low Mask (ϕ)	Disable the trigger with ϕ 3-station or 2-station coincidence
R-ϕ Dummy	Allow to issue the trigger with no wire or strip coincidence
p_T Mask	Disable specified p_T level

Table 7.6: Special Mask

7.5.2 Input Checker

This function monitors the input pattern from the HPT module. G-Link data consists of 16 bits of Word Field and 4 bits of Code Field in a row. The row of these fields is locked by the serial to parallel converter HDMP1034. But there is some possibility to lock at a wrong point. In normal usage, G-Link should be set in Idle mode if it have no communication. But the case of SL, the process must be operated without deadtime. Therefore the communication mode is fixed in Data mode. If the wrong locking is occured, known invalid patterns will be issued from HDMP1034. If Input Checker finds invalid pattern for 32 clock continuously, send a request to execute the Recovering Procedure (Section 7.2.3.1) to G-Link Monitor. This type of error can be detected by only Main FPGA because G-Link Monitor has no connection of data line from HDMP1034.

7.5.3 Scaler

Scaler is of a monitoring function in the logic of Main FPGA. This is a kind of counters for many purpose. An internal timer module is implemented and it sends the reset signal for every 400M clocks. Scaler counts the number of trigger in the trigger counters until receiving a reset signal from the timer. When Scaler receives the reset signal, the Scaler writes a counted number to registers, and flash the

trigger counter. Counted registers keep the number of trigger in previous 400M clocks until receiving the next reset signal.

- Input Scaler: Count the number of input signal in each input connectors.
- SSC Scaler: Count the number of trigger candidate in each SSC module.
- Trigger Scaler: Count the number of L1A candidate.

7.5.4 Mask

Mask function is mainly used for module test and commissioning period. This function enables us to control the trigger setup through VME communication. It is easier to change the trigger setup through VME than preparing new bitmap file.

- H/L Mask : Reject an input from HPT if its coincidence level is 2-station station
- SSC Mask : Block off an SSC to issue any trigger candidate.
- Trigger Stopper : Stop trigger immediately if its rate exceeds the limit. Trigger is blocked until receiving the next reset signal from timer module (same timer as mentioned in section 7.5.2). The limit can be changed through VME.

These are prepared because HPT modules do not have any blocking functions. If upper modules (for example, PSB) goes crazy, HPT may issue many empty triggers. It will crash the ATLAS data taking. Even if this problem cannot be fixed soon, TGC must come back the data taking as quickly as possible. The problematic region will be masked out by this function.

7.6 Validation of Sector Logic

Validation of the process of SL is mandatory for the stable operation for LVL1 Endcap Muon System. In this section, the result of such validation for SL is presented. The item of studies are listed in Table 7.7, and the data which is used to validate the SL process is described in following list in Table 7.8. Here the Front End indicates 2-station coincidence and 3-station coincidence data, while SL data indicates the issued LVL1 Endcap Muon Trigger.

It is confirmed SL trigger has parents of wire and strip pair.
When a pair of wire coincidence and strip coincidence which must be triggered are found, it should confirmed whether SL provided a trigger or not.

Table 7.7: Check Items of Validation

Run#158045 (pp collision run in 2010)
Number of Front End data (the total of wire and strip) : 215,280
Number of SL data : 133,357

Table 7.8: Used Statistics for Validation

Both directions of Front End and SL data must be compared. In validation for issued p_T level is confirmed with database file and ucf file. It means triggered data are compared with Coincidence Window and LUT of implemented in FPGA.

7.6.1 Validation of Sector Logic to Front End

Purpose of this validation is to confirm the trigger source of SL. SL trigger must have a pair of wire coincidence and strip coincidence. The requirements of SL validation are;

Find an SL trigger and search a pair of wire-strip coincidence in the same BCID as SL. This pair is selected because they can be make an ROI, and it is compared with the trigger ROI which is issued from S
The reference p_T level which should be issued by wire-strip pair is retrieved from .db file and .ucf file. And they are compared with the p_T level which is issued by SL.

At the result, it was confirmed that all SL trigger has wire-strip parents are found. The triggering algorithm which is implemented in SL is working correct.

7.6.2 Validation of Front End to Sector Logic

If a pair of wire coincidence and strip coincidence which can be make a trigger candidate was found, then SL must issue a trigger but the robustness of SL process have not been confirmed. This validation analysis will confirm about validation what SL issued a trigger or not. The validation requirements and methods are;

- Wire and strip information are searched. When wire information is found, search a strip information which can make a trigger candidate. If a wire-strip pair is found, this will be validation reference. A position information of ROI is determined using the wire-strip pair, and the reference's p_T level, which retrieved from .db file and .ucf file, is determined.
  if more than 2 references are found in each trigger sector, then up to two highest priority candidates will be selected. The priority rule is described in previous chapter "Endcap".

- Search the SL trigger which contains of same ROI as a reference.

- If a trigger which contains same ROI as a reference's information, then the p_T threshold is compared between trigger and reference.

At the result, problematic case could not be found in this validation. It was validated that the Sector Logic issues the correct LVL1 trigger candidates.

Chapter 8

Performance Studies

LVL1 Endcap Muon Trigger system (TGC chambers and trigger electronics) was installed by the end of 2007 and has been working for beam collision at LHC. It is important to validate the trigger system and evaluate its performance of LVL1 Endcap Muon Trigger for the experimental result of ATLAS.

In this chapter, the performance for the latest setup of the LVL1 Endcap Muon Trigger system is described. First, the detail of Coincidence Window for the latest setup is described. Then, measurements of efficiencies are explained. At the last, purity of the trigger is discussed together with trigger rate and sources of fake triggers.

8.1 Coincidence Window

In this section, the detail of the Coincidence Window for the beam collision is described. The coincidence window is prepared based on the Monte Carlo simulation. First, simulation scheme is described. Next, how to make the Coincidence Window from the simulation data is explained. At last, cross-talks in TGC chambers together with its effects on the Coincidence Window is discussed.

8.1.1 ATLAS Simulation Scheme

The Coincidence Window is generated using ATLAS detector simulation.

The ATLAS simulation consists of mainly four processes; event generation, detector simulation, digitization, and reconstruction. Figure 8.1 shows the processing procedure of ATLAS simulation. The event generation part makes collision events (i.e. all particles at the collision point with their

energy, and momentum) by using monte carlo simulation of some physics model. The detector simulation part reproduces interactions between particles and detector materials using Geant4 [37] of a tool kit for detector simulation. All primary and secondary particles are tracked inside the ATLAS detector and information such as position, time, momentum and energy deposits in the detector are recorded (called as G4Hits). Detailed detector shapes and magnetic fields inside are described. Based on the track information from detector simulation, the digitization part emulates detector responses including front-end and readout electronics. Emulation of LVL1 Endcap Muon Trigger System is included in this part. The format of outputs from digitization (called as G4Digit) is basically same as one for the real ATLAS experiment. Final part is reconstruction, where information of the particles at the collision point are reconstructed by using the digitized data. The output is called as ESD (Event Summary Data), which is input for further analysis.

The emulator of LVL1 Endcap Muon Trigger system is implemented in the last part of digitization. It receives hit information of ASDs from the digitizer for TGC chambers. Each module of LVL1 trigger system, such as SLB, HPT and SL, are emulated in detail. Coincidence Window is generated by using emulated HPT outputs (i.e. δR, $\delta\phi$) and true p_T of the muon track.

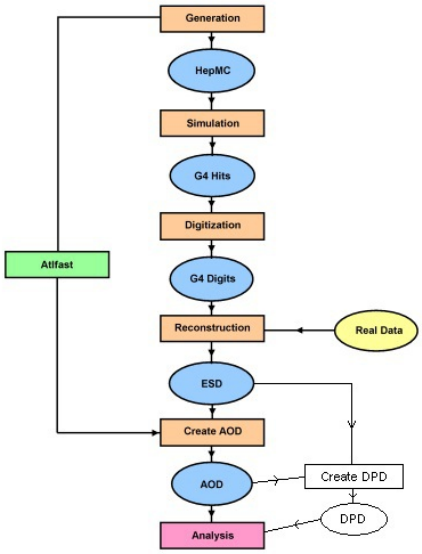

Figure 8.1: Full Data Chain

p_T threshold	Trigger Name	Requirements & Target
1	L1_MU4	Requires 2 station coincidence without specific region.
2	L1_MU6	Requires 3 station coincidence, target track is muon with more than 6GeV
3	NA	RPC Special Trigger
4	L1_MU11	Requires 3 station coincidence, target track is muon with more than 10GeV
5	L1_MU15	Requires 3 station coincidence, target track is muon with more than 15GeV
6	L1_MU20	Requires 3 station coincidence, target track is muon with more than 20GeV

Table 8.1: LVL1 Endcap Muon Trigger Menu at the end of 2011

8.1.2 Production of Coincidence Window

For physics runs in the autumn 2011, the Coincidence Window was prepared with p_T thresholds shown in Table 8.1. It is difficult to describe a simple formula between observed sagitta and track p_T because magnetic fields are complex in the endcap region. Thus Coincidence Window is generated using simulation data for single muon events, where only one muon from the interaction point is included in each event. A hitmap for each ROI is prepared by using single muon samples. A hitmap can be visualized by a two-dimensional histogram as shown in Figure 8.2 and 8.3. It is a list of number of entries of muons on δR-$\delta\phi$ space for each ROI.

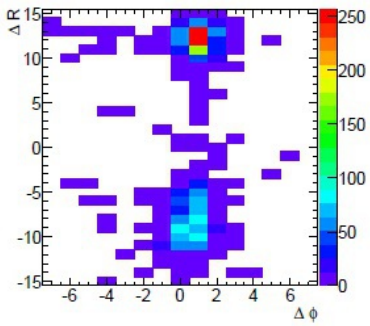

Figure 8.2: Example of Hitmap, generated by single muon with p_T = 6GeV/c

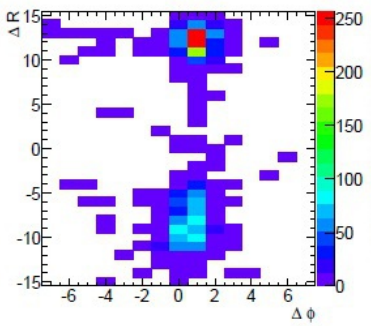

Figure 8.3: Example of Hitmap, generated by single muon with p_T = 10GeV/c

Hitmaps are prepared for following single muon samples; p_T = 6GeV/c, 8GeV/c, 10GeV/c, 15GeV/c, 20GeV/c, 40GeV/c, and 100GeV/c. Coincidence Window for each p_T threshold is prepared with samples with threshold p_T and higher p_T; for example, hitmaps for 10GeV/c and 15GeVGeV/c

are merged to create the Coincidence Window for 10GeVGeV/c p_T threshold. This merged hitmap can represent a hitmap for continuous p_T distribution. Cells are added one by one for a certain p_T threshold according to the following rules, where the cell is defined as each bin in δR-$\delta\phi$ plane. Cells are added until the sum of entries in opened cells reaches to 95% of total number of entries in the hitmap. Then, opened cells for all p_T thresholds are superimposed. Here, cells for higher p_T thresholds take precedence. At last, cells which have no other opened cells around are removed, and not-opened cells which are surrounded by other opened cells are additionally opened. There are 1080 kinds of Coincidence Windows prepared for 2011 runs; 888 for 6 Endcap sectors and 192 for 3 Forward sectors. These sectors correspond to one octant because the magnetic field in ATLAS has 8-fold symmetry. There are some differences between each octant in detail, but set of Coincidence Windows which generated for an octant is applied for all octants.

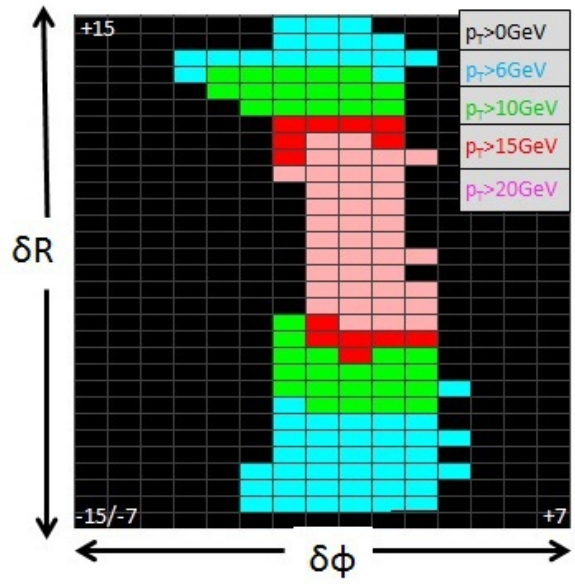

Figure 8.4: Example of Visualized Coincidence Window: x axis means $\delta\phi$, y axis means δR. Center of axis indicates 0 of delta value. δR has the width of $\pm$15, $\delta\phi$ has the width of $\pm$7.

8.2 Effects of TGC crosstalk

As described before, the Coincidence Windows are prepared by using Monte Carlo simulation. If simulated chamber response differs from the real one, the effects should be taken into account.

Crosstalk effect in chambers has been observed. Hits appears in several neighboring channels for one charged tracks. This effect is more remarkable for strip channels than for wire channels. If crosstalk of strip channels occur, $\delta\phi$ measured by HPT could be different from the true one as shown in Figure 8.5[1]. It is found that the trigger efficiencies degrade about 8% compared to the simulation data because of this crosstalk effects as shown in Table 8.2.

In this section, origin of crosstalk and effects on the δR and $\delta\phi$ measurements are described. At last, we explain modification of the Coincidence Window to overcome this effect.

	Monte Carlo	Beam Data
L1MU0	0.965 ±0.001	0.960 ±0.009
L1MU6	0.945 ±0.001	0.875 ±0.014

Table 8.2: Trigger Efficiency in the early period of LHC beam collision (without the cross talk effect)

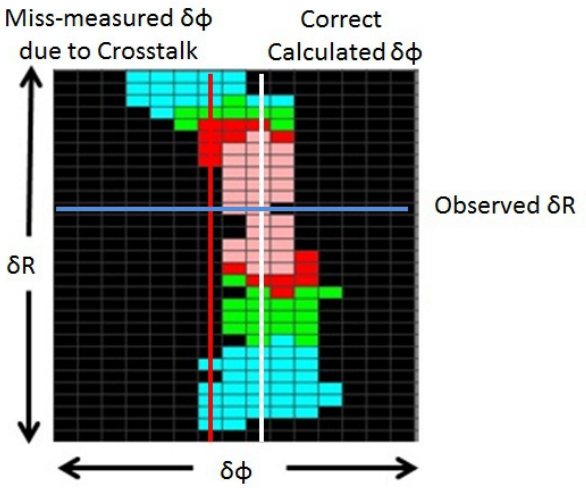

Figure 8.5: Example of effect of crosstalk: Blue line is observed δR, white line is collect $\delta\phi$, red line is observed wrong $\delta\phi$. The pink colored cell at crossing of blue and white lines should be selected. Due to the crosstalk effect, the black cell at crossing of blue and red lines is used and no trigger will be issued.

8.2.1 Origin of Cross Talk

Crosstalk on wire channels occurs, if a muon track passes through the boundary region of adjacent wires. Signals on strips are caused by induced charge via capacitance between strips and the

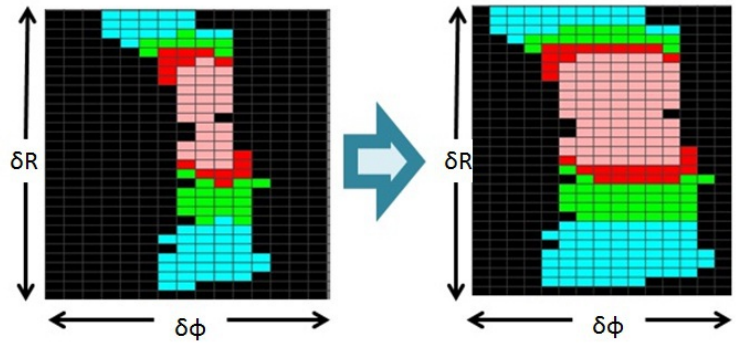

Figure 8.6: Modification of the Coincidence Window for Crosstalk Effect. Left side picture shows the Coincidence Window with no crosstalk effect, and right side picture shows the modified Coincidence Window for fixing the problem of crosstalk

avalanche point. So, crosstalk on strip channels can occur for large signals as well as for boundary region of adjacent strips. In addition, crosstalk on strips can occur via capacitance between wire and strip because decoupling capacitance for wire channels is not so large (498pF) compared to detector capacitance (100-200pF).

Therefore, crosstalk on strip channels is severer than one on wires. The effect is more remarkable for chambers at higher η region because strips are narrower and portion of boundary region against the overall area is larger.

8.2.2 Declustering Rule

In HPT, the $\delta\phi$ is measured by using position information of SLB coincidences of doublets and triplets. Crosstalk effect on triplets is most remarkable because SLB coincidence for triplets is simple OR logic between two layers. The hit positions are sent from the SLB coincidence for triplet strips. In case that neighboring channels have hits, the position is determined according to the following declustering rule. The primary hit channel in a cluster will be the second lowest number of hit channels. An example of cluster size and readout hit position is described in Figure 8.7.

8.3 Effect of Dead Chambers

Some TGC chambers have problems; noisy channels, or dead channels. Noisy channels with high occupancies may make fake triggers and/or trigger dead time because of increase of readout time.

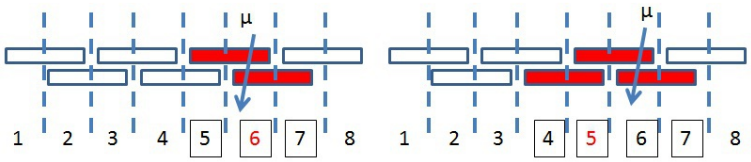

Figure 8.7: Declustering Rule with Effect of Crosstalk. Each strip channel is shown as a box and hit channels are colored with red. The left picture has no crosstalk and the right one has crosstalk hits. The numbers below indicate position of coincidence. The numbers in box are hit channels and red one is the selected position as a result of declustering.

So, noisy channels are masked off at inputs of SLB. Noisy channels and dead channels may result in trigger hole. Especially, dead chambers, to which high voltage can not applied, and dead ASDs are crucial because they cause large insensitive area. To avoid making any trigger hole, dummy hits are filled up at coincidence inputs of SLBs. However, dummy hits can not be applied to triplet strips. Dummy hits cause consecutive coincidence hits because of 1 out of 2 coincidence is required in triplet strip. For such a place which cannot be filled up with dummy hits, a special Coincidence Window is applied for L1_MU6 and L1_MU10. They can be issued even for 2-station coincidence though 3-station coincidence for both wire and strip is required in default. This special Coincidence Window is also applied if more than one layers are dead out of 3 wire layers in a triplet. Now there are two of trigger sectors in Forward have such a problematic chamber.

8.4 Measurement of Efficiencies

Measurement of trigger efficiencies is important to study performance of LVL1 Endcap Muon Trigger. Trigger efficiency $\epsilon_{trigger}$ is defined as

$$\epsilon_{trigger} = \frac{N_{triggered}}{N_{track}} \tag{8-4-1}$$

,where N_{track} is number of muon tracks in endcap region and $N_{triggered}$ is number of muons with matched LVL1 trigger.

8.4.1 Combined Muon

A muon created in beam collision is reconstructed by using various subsystems in ATLAS detector. There are two kinds of muon tracking, one is standalone muon track, and the other is combined muon

track. Standalone muon track is reconstructed with whole muon spectrometers. Combined muon track is reconstructed with inner detectors and standalone muon tracks. If an inner detector track is matched with standalone muon track, a combined track is made from these two tracks.

ATLAS has several kinds of combined muon tracking algorithm, the two of major algorithms are named STACO (Statistical Combined) and MuID (Muon Identification). In this paper, combined tracks by STACO are used for further analysis.

8.4.2 Tag and Probe Method

Tag and Probe method is adopted for measurements of trigger efficiencies. This method can be applied for events with a decay into two muons as shown in Figure 8.8. First, each reconstructed muon is examined whether it is triggered or not according to a method described later.

If it is triggered, the muon is named a tagged muon. Second, another muon, which has opposite charge, is searched for. The invariant mass of the tagged and second muons is examined. If the mass is matched to the parent particle mass, these muons can be considered as decay products. Thanks to reconstruction of the decay, purity of the reconstructed muon is fairly good. The second muon track from the di-muon decay is called as probe muon. The probe muon is examined to have matched trigger or not. In calculation of trigger efficiencies, the denominator , N_{track}, is the number of probed muons and the numerator, $N_{triggered}$, is the number of probed muons with matched trigger. In this analysis, events have been triggered by the tagged muon. So, no bias in measurements of efficiencies is expected.

In this thesis, $Z \rightarrow \mu\mu$ decays is used for measurement of efficiencies. The mass of Z boson (M_Z) is 91.2 GeV [38] and muons from this decay has high p_T. Selection criteria for Z decay events is shown in Table 8.3. Z_{pv} is the primary vertex on z coordinate, $M_{\mu\mu}$ is the reconstructed mass of di-muon.

Criteria for muons (muon selection, tag and probe selection) are listed in Table 8.4, 8.5, and 8.6. N_{pv} is number of charged tracks from the primary vertex. Following requirements are applied to the track reconstructed in the inner detectors. N_{pixel} is the number of hits of the reconstructed track in Pixel Detector, $N_{pixelblayer}$ is the number of hits of the track on b-layer of Pixel detector, $N_{DeadPixel}$ is the number of dead pixel sensors which the track passes through. $N_{PixelHole}$ is the number of holes of Pixel detector, N_{SCT} is the number of hits of the reconstructed track in SCT, $N_{DeadPixel}$ is the number of dead pixel sensors which the track passes through, $N_{SCTHole}$ is the number of holes of SCT. $N_{TRT} = N_{TRTHit} + N_{TRToutlier}$, N_{TRTHit} is the number of TRT hits of the reconstructed track in

TRT, and $N_{TRToutlier}$ is the number of hits on TRT but these hits are away from offline track. Δz_0 is differencies of z coordinate of tag muon and probe muon, Δd_0 is the differencies on *x*-*y* coordinates between tag muon and probe muon. ΔR is the distance between offline track and trigger ROI, which can be described like $\sqrt{\Delta\eta^2 + \Delta\phi^2}$, where $\Delta\eta$ is differencies between ROI η and offline track η, and $\Delta\phi$ is differencies between ROI ϕ and offline trackϕ. EF_$mu18_medium$matching is a trigger menu on Event Filter. This trigger is seeded by L1_$MU10$ at the stage of LVL1 trigger, and L2_$mu18_medium$matching at the stage of LVL2 trigger. The matching between offline track and muon trigger is required $\delta R < 0.15$. This area is wider than the area of ROI on $\eta - \phi$ plane, for example, the area of endcap ROI is approximately 0.04 and forward is 0.07. Reconstructed mass distribution is shown in Figure 8.9. Its peak is 90.93 ± 0.03 GeV/c^2.

$\lvert Z_{pv}\rvert < 150mm$
$\lvert M_{\mu\mu} - M_Z\rvert < 10GeV/c$

Table 8.3: Z Requirements

Vertex Cut
$N_{pv} \geq 3$
Inner Detector Cut
$N_{Pixelblayer} > 1$
$N_{Pixel} - N_{DeadPixel} > 1$
$N_{SCT} - N_{DeadSCT} > 5$
$N_{PixelHole} + N_{SCTHole} < 2$
$N_{TRT} > 5$ and $\frac{N_{TRTout}}{N_{TRT}} < 0.9$ (if $\lvert\eta\rvert < 1.9$)
$\frac{N_{TRTout}}{N_{TRT}} < 0.9$ (if $\lvert\eta\rvert \geq 1.9$ and $N_{TRT} > 5$)

Table 8.4: Muon Requirements

Muon Requirements+
$Track p_T > 20\text{GeV}$
$\lvert\eta\rvert < 2.4$
$\lvert z_0 - z_{pv}\rvert < 10mm$
$\frac{\Sigma p_T(\Delta R<0.2)}{p_T} < 0.1$
$withEF\_mu18\_medium$ matching

Table 8.5: Tag Muon Requirements

Muon Requirements+
Has opposite charge of tagged muon
$\lvert\eta\rvert < 2.4$
$\lvert z_0 - z_{pv}\rvert < 10mm$
$\frac{\Sigma p_T(\Delta R<0.2)}{p_T} < 0.1$
$\lvert\Delta\phi_{Tag-Probe}\rvert > 0.2$
$\Delta z_0 < 3mm$
$\Delta d_0 < 2mm$

Table 8.6: Probe Muon Requirements

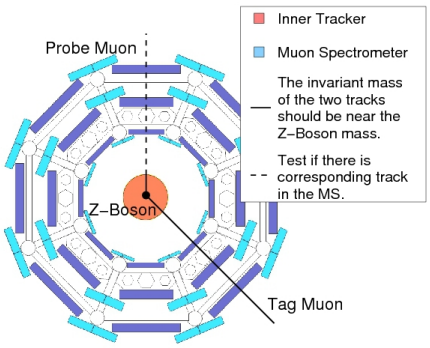

Figure 8.8: Tag and Probe Method

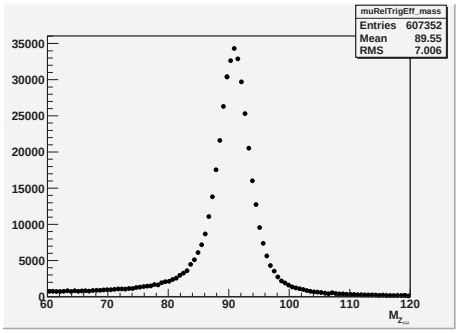

Figure 8.9: $M_{\mu\mu}$ Distribution, horizontal axis means the reconstructed mass of Z (GeV/c^2)

8.4.2.1 Distributions of Probe Muons

In this analysis, used statistics are shown in Table 8.7.

Figure 8.10, is the distribution of probe muons on η coordinate. This distributions, especially around the boundary of barrel, effect of the structure of inner detectors can be seen. It is difficult to reconstruct the muon track on $|\eta|$=1.2, because this is the barrel-endcap boundary of inner detectors. Figure 8.11 is the distribution of probe muons on ϕ coordinate. This distribution shows the effect of supports of the ATLAS detector. Support structures locate in the region of $\phi \approx$-1 and $\phi \approx$-2 in the barrel. Di-muon from Z decay have tendency to go back to back in R-ϕ plane. If a muon flies into support area where no muon detectors are installed, it is difficult to reconstruct an offline track. Thus another muon which flies into opposite side ($\phi \approx 1$ and $\phi \approx 2$.) is difficult to to be identified as to be a probe muon. Figure 8.12 is the distributions of probe muons on reconstructed p_T. Its peak locates near by the half of M_z.

Probe Muon	190,156
Matched Muon	177,664

Table 8.7: Statistics of Tag and Probe

Distributions of matched muon $p_T$is shown in Figure 8.13. The trigger with lower thresholds contain the events taken by high-threshold triggers. For example, L1_MU4 contains L1_MU4 to L1_MU20.

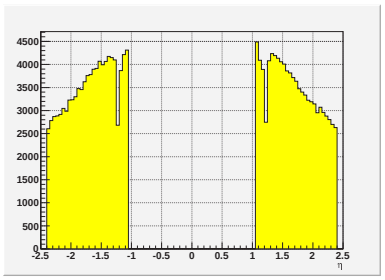

Figure 8.10: Probe Muon (η): This is the η position distribution of probe muon

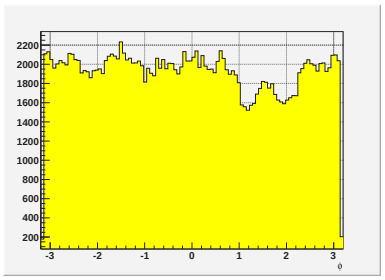

Figure 8.11: Probe Muon (ϕ): This is the ϕ position distribution of probe muon

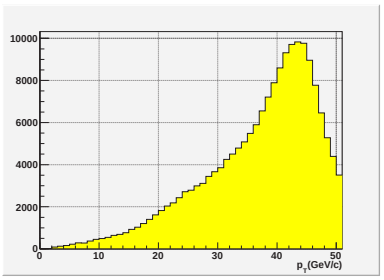

Figure 8.12: Probe Muon p_T: This is the p_T distribution of probe muon(GeV/c)

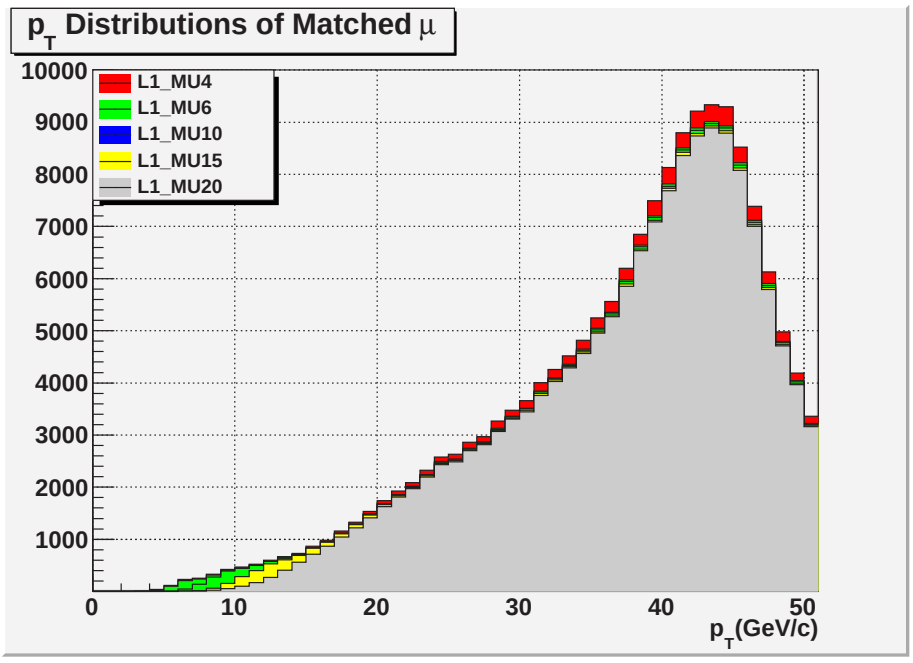

Figure 8.13: The Distributions of Matched Muon p_T for each p_T level. Horizontal axis means the offline muon p_T(GeV/c)

8.4.2.2 Trigeger Efficiency

Trigger Efficiency of LVL1 Endcap Muon Trigger is measured as a function of p_T, η and ϕ.

The η and ϕ dependence of trigger efficiencies for L1_MU4 are shown in Figure 8.14 and 8.15, respectively. Black and red markers indicate data, and simulation results, respectively. Efficiencies are kept high over all endcap region. Small position dependences can be seen, but simulation agrees very well with the data as shown in Figure 8.21 and 8.22. So, these dependences are considered as effects of detector geometry.

Trigger efficiencies for each p_T threshold are shown as a function of p_T in Figure 8.16 to 8.20, these figures shows the trigger efficiency for each p_T level, and their horizontal axis means the p_T(GeV/c) of offline track. Efficiencies rise up at different p_T according to threshold level. Agreements between data and simulation are fine as shown in Figure 8.23 to 8.27, their horizontal axis means the offline track p_T as same as Figure 8.16 to 8.20. Each distribution is fitted by using the formula;

$$\epsilon_{trigger} = \frac{\epsilon_{plateau}}{1 + e^{-\frac{1}{width}(p_T - Th)}} \tag{8-4-2}$$

where $\epsilon_{plateau}$ (plateau efficiency) indicates maximum efficiency, Th indicates threshold momentum, and width indicates momentum resolution.

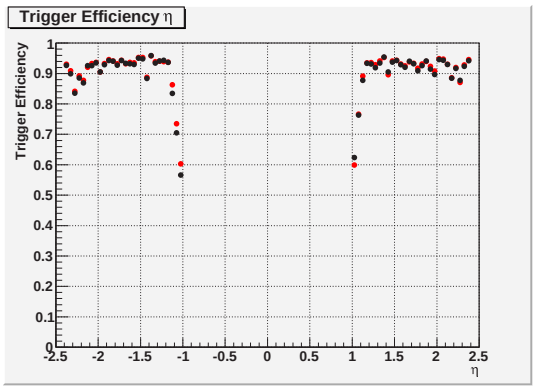

Figure 8.14: Trigger Efficiency vs η. Black and red markers indicate real data, and simulation results, respectively.

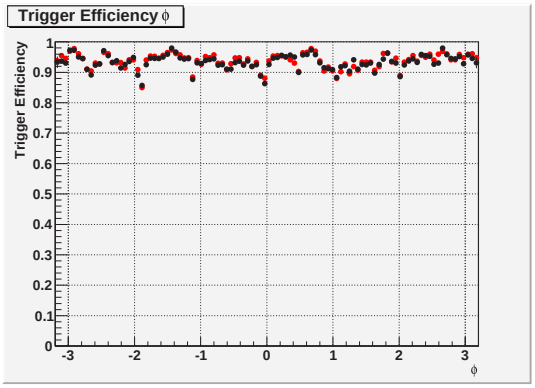

Figure 8.15: Trigger Efficiency vs ϕ.

Trigger efficiency between data and simulation is compared. Following histograms are made on $\epsilon_{simu} - \epsilon_{data}$. All differences are small, each histograms are within ± 0.1.

Trigger Menu	ϵ_{MC}	ϵ_{Data}
L1_MU4	0.956 ± 0.001	0.949 ± 0.001
L1_MU6	0.919 ± 0.001	0.915 ± 0.001
L1_MU10	0.914 ± 0.001	0.911 ± 0.001
L1_MU15	0.908 ± 0.001	0.904 ± 0.001
L1_MU20	0.903 ± 0.001	0.898 ± 0.001

Table 8.8: Trigger Efficiency at plateau region for each p_T threshold

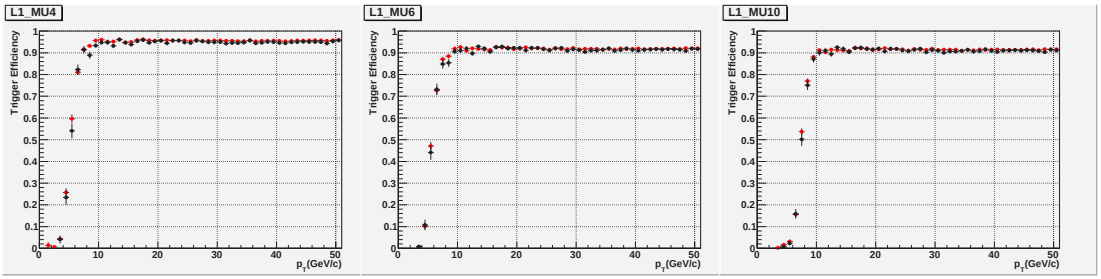

Figure 8.16: Efficiency vs p_T, L1_MU4.

Figure 8.17: Efficiency vs p_T, L1_MU6.

Figure 8.18: Efficiency vs p_T, L1_MU10.

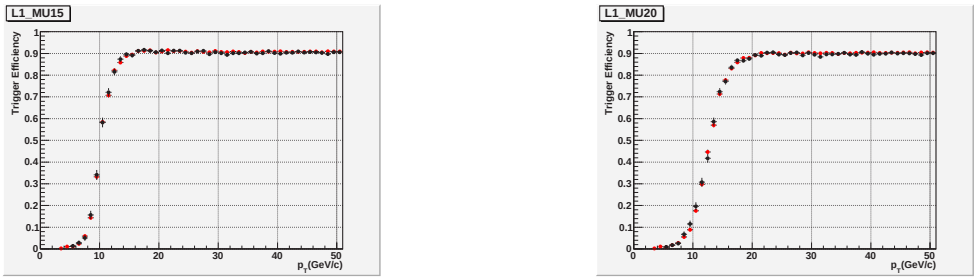

Figure 8.19: Efficiency vs p_T, L1_MU15.

Figure 8.20: Efficiency vs p_T, L1_MU20.

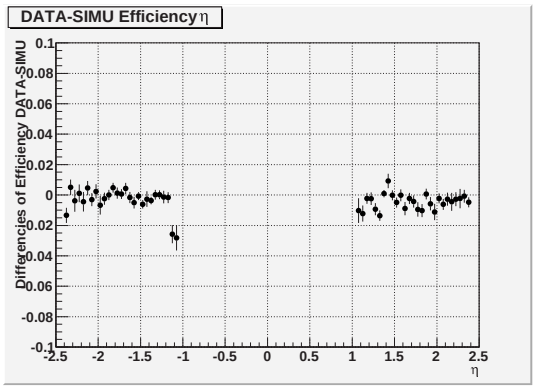

Figure 8.21: Differencies of Trigger Efficiency η

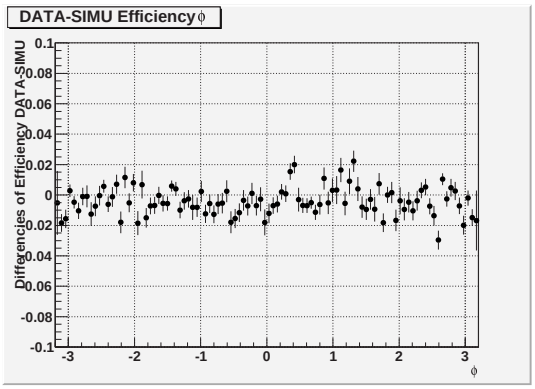

Figure 8.22: Differencies of Trigger Efficiency ϕ

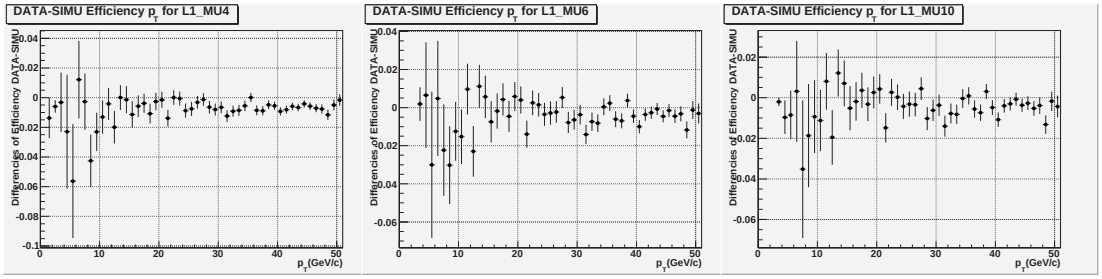

Figure 8.23: Differencies of Trigger Efficiency L1_MU4

Figure 8.24: Differencies of Trigger Efficiency L1_MU6

Figure 8.25: Differencies of Trigger Efficiency L1_MU10

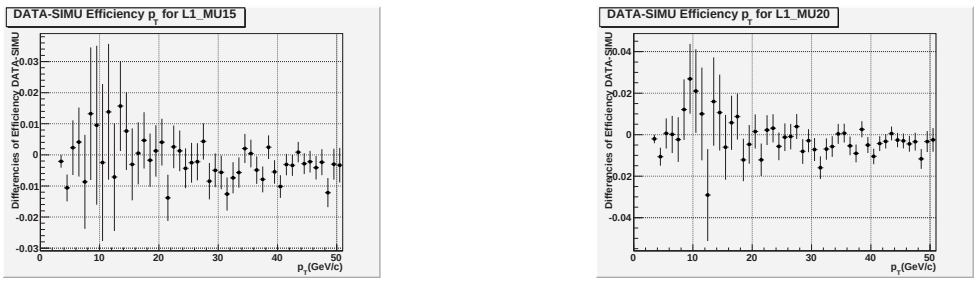

Figure 8.26: Differencies of Trigger Efficiency L1_MU15

Figure 8.27: Differencies of Trigger Efficiency L1_MU20

8.4.3 Trigeger Timing

Timing of LVL1 Endcap Muon Trigger is examined for events with calorimeter trigger. In Figure 8.28 shows fraction of events as a function of time difference between muon and calorimeter trigger in unit of bunch clock. Black histogram shows fraction for all muon trigger. Blue and red histograms are fraction with and without combined muon matched to the muon trigger, respectively. Muon triggers are issued at the correct timing for most of events with matched combined track. Fake triggers without an offline muon come from cavern background, protons coming from beam pipe and so on.

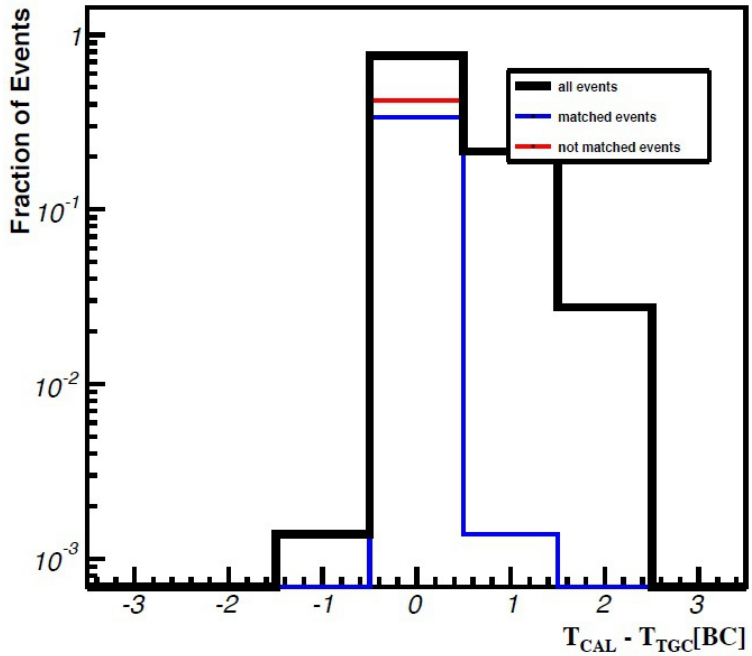

Figure 8.28: Trigger Timing compared with calorimeter. Horizontal axis means the difference between BCID on calorimeter trigger and BCID on LVL1 Endcap Muon Trigger(TGC), vertical axis means the fraction of events. Except the bin which indicates 0, red colored histogram is covered by black histogram because almost of all entries are dominated by red entry.

8.5 Fake trigger

In the pp collision period at the end of 2011, trigger rate for L1_MU11 reached 8.19kHz, In 75kHz of total LVL1 rate, 15kHz is assigned to muon triggers. For 2012 and further, running higher luminosity of LHC is expected and it will result in higher trigger rate if without changes in trigger condition. So, it is very important to improve purity of trigger within minimum efficiency loss.

Element of Study	Number of Events
L1_MU11	14720
Offline Muon	5215
p_T > 10GeV	766

Table 8.9: Number of L1_MU11, triggered offline muons, and offline muon which has p_T > 10GeV

As described before, there are many fake triggers without matched muons. Endcap Muon Trigger use TGC hits only in big wheel and momentum measurement can work correctly only for tracks coming from the interaction point. So, it is difficult to avoid triggering a fake track if it does comes from beam collision but it points to the interaction point after toroidal magnetic field. In this section, origin of fake triggers is discussed together with their rate.

In Figure 8.29, black line shows η distribution of triggered ROI for L1_MU11. Data taken by L1_MU11 without no further selection in higher level trigger (i.e. trigger menu is EF MU11 NoAlg) in run #190343 is used. The combined track is examined for each ROI. ROIs with matched combined muon are shown in Blue histograms. Yellow histogram shows ROIs with p_T >10 GeV/c.

ROIs which matched with offline muons have found 35.4%. Especially, ROIs which matched with offline muons more than p_T >10GeV have found 5.2%. Among triggers in the endcap region, 64.6 % are fake and have no matched track.

A study on fake triggers in the endcap region reveals that most of fake tracks have slow velocity and no corresponding hits in the small wheel in front of the endcap toroidal magnets. We guess that they are hadrons coming from the wall of endcap troidal magnets.

So, if TGC trigger is required wire-strip hit on EI/FI at the coincidence step of SL, trigger rate of L1_MU11 will be reduced to 81.0% and trigger efficiency will be kept over 90%. This method will provide higher quality L1_MU trigger, and reduce the trigger rate.

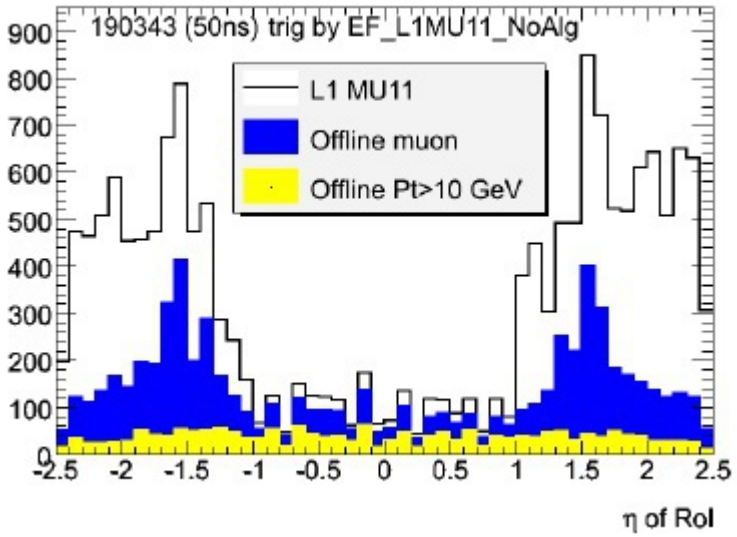

Figure 8.29: Distributions of $L1\_MU11$ and offline muon track on η direction. Black plot shows all events of $L1\_MU11$ trigger, blue plot shows the distribution of $L1\_MU11$ which matches with offline muon track, and yellow plot shows $L1\_MU11$ trigger with matched offline muon track which has more than 10GeV/c transverse momentum.

Chapter 9

Summary

Trigger algorithm on electronics is validated and SL is working with no error. The performance of trigger algorithm is studied. Especially, it was validated that the performance of an electoronics of Sector Logic. The implemented algorithm works fine, and Sector Logic performed flexibility of copes to fix any problem and satisfy requirements from ATLAS group. LVL1 Endcap Muon Trigger has been operated stably in 2011 electoronics. Individual Coincidence Window have been applied for each Trigger in order to remedy problematic regions where dead chambers and/or noisy channels were found.

The performance of LVL1 Endcap Muon Trigger is studied using Tag and Probe method with $Z \rightarrow \mu\mu$ production. No dead region in η and ϕ coordinates are found. It is confirmed that the high efficiency trigger with more than 90% in each p_T threshold. The consistency of trigger timing with offline muon track is studied. A trigger without offline muon track is dominantated by out-bunch events. It is found that most of tracks triggered by L1_MU11 but without offline muon come from the beam pipe. To get rid of fake triggers, method of using inner TGC stations was proposed. If hits on EI/FI are required on the coincidence stage of SL, the fake trigger will be reduced about 20%.

ATLAS experiment already issued many physics result. Ofcourse LVL1 Endcap Muon Trigger contributed the research of Higgs boson [39].

Several mass regions are already limited on 95% coinfidence level for searching Higgs. This research considered some decay channels which contains muon analysis. This is an important contribution of LVL1 Endcap Muon Trigger. Figure 9.1 is the result of ATLAS 2011.

The update to reduce the trigger rate which are associated with no offline muon track will be needed. But LVL1 Endcap Muon Trigger will be overcome any problems and contribute the ATLAS

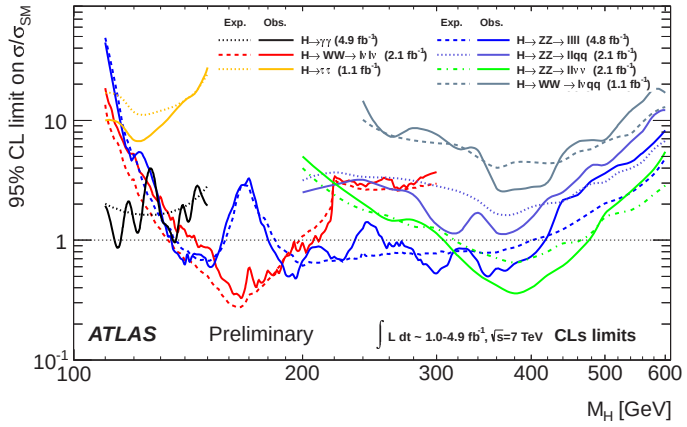

Figure 9.1: 95% Confidence Level Limits on $\sigma_{Higgs}/\sigma_{SM}$

experiment to provide the high quality LVL1 trigger.

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